Change Summary

CHANGES

No.	Applicable Section	Description	Page(s)
1	Electrical Characteristic	Updated	5-8
2	General description	Updated	2
3	Functional description	Updated	10,11,13,15
4	Typical application schematic	Updated	28
5			
6			
7			
8			

REVISION HISTORY

Revision No.	Description of change	Release Date
0.5	Initial release	2017/12/05
0.7	Updated #1	2018/03/12
0.71	The changes are listed above from #2 to #3,#4	2018/05/09

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I²C Controlled 3A Fully Integrated 1 Cell Li-Ion Battery NVDC Charger with MPPT control for Solar Panel

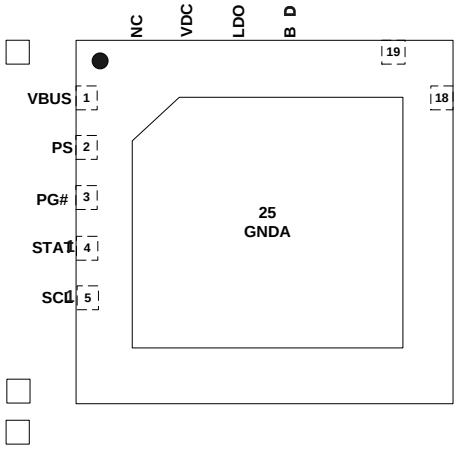
FEATURES

- High accuracy switched mode 1 cell Li-Ion charger with integrated synchronous switching MOSFETs
- Support Intel NVDC topology
- Support Quick Charge, VBUS input voltage up to 14V
- Support VINDPM mode to set the MPPT voltage using for solar panel power
- Input current optimization function to identify the maximum input power to not overload
- Dynamically allocates USB input power including input voltage regulation and input current limit to adapt all kinds of adapter
- Constant ripple current (CRC) control and no external loop compensation
- Integrated charging sensing resistor and input current sensing resistor
- Integrated bootstrap diode
- Support USB 2.0, 3.0 USB Standards and higher voltage adapter
- Setting charging current from 0A to 3A
- Integrated 15mΩ battery discharge MOSFET up to 9A pulse discharge current to get highest battery discharging efficiency
- I²C programmable battery path impedance compensation to accelerate charge time
- Up 93% charge efficiency at 2A and 91% at 3A
- I²C setting and battery charge management
  - ±0.5% voltage mode accuracy
  - ±5% current mode accuracy
  - ±3% VBUS input voltage limit accuracy
- 100mA to 3.25A input current limit
- VBUS UVLO and Over-Voltage Protection, VSYS Over-Voltage Protection
- Power MOSFETs Over-Current Protection
- Support shipping mode
- Joint Power Supply when system over load
- Support autonomous battery charging process without I²C communication
- Provides telemetry and charging status indication information via I²C(voltage, temperature, current)
- Interrupt output IRQ to host
- Thermal regulation and Over Temperature Protection
- Charger safety timer
- Low battery current dissipation when only battery present
- Lead free and RoHS Compliant

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ1C82	-40°C to 125°C	QFN24, 4mmx4mm

PIN DIAGRAM



APPLICATIONS

- Shared bike
- Cell Phone
- Other Solar Panel devices

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GENERAL DESCRIPTION

OZ1C82 is an I^{2}C controlled power management IC for single cell LiIon or Li-polymer battery systems in a wide input range of Solar panel powered devices, like shared bike, power bank or other portable device.

OZ1C82 supports all kinds of input sources (type) range is from 3.9V up to 14V in operation, which is very suitable for solar panel application since the solar panel voltage is variable with different weather ere

BLOCK DIAGRAM

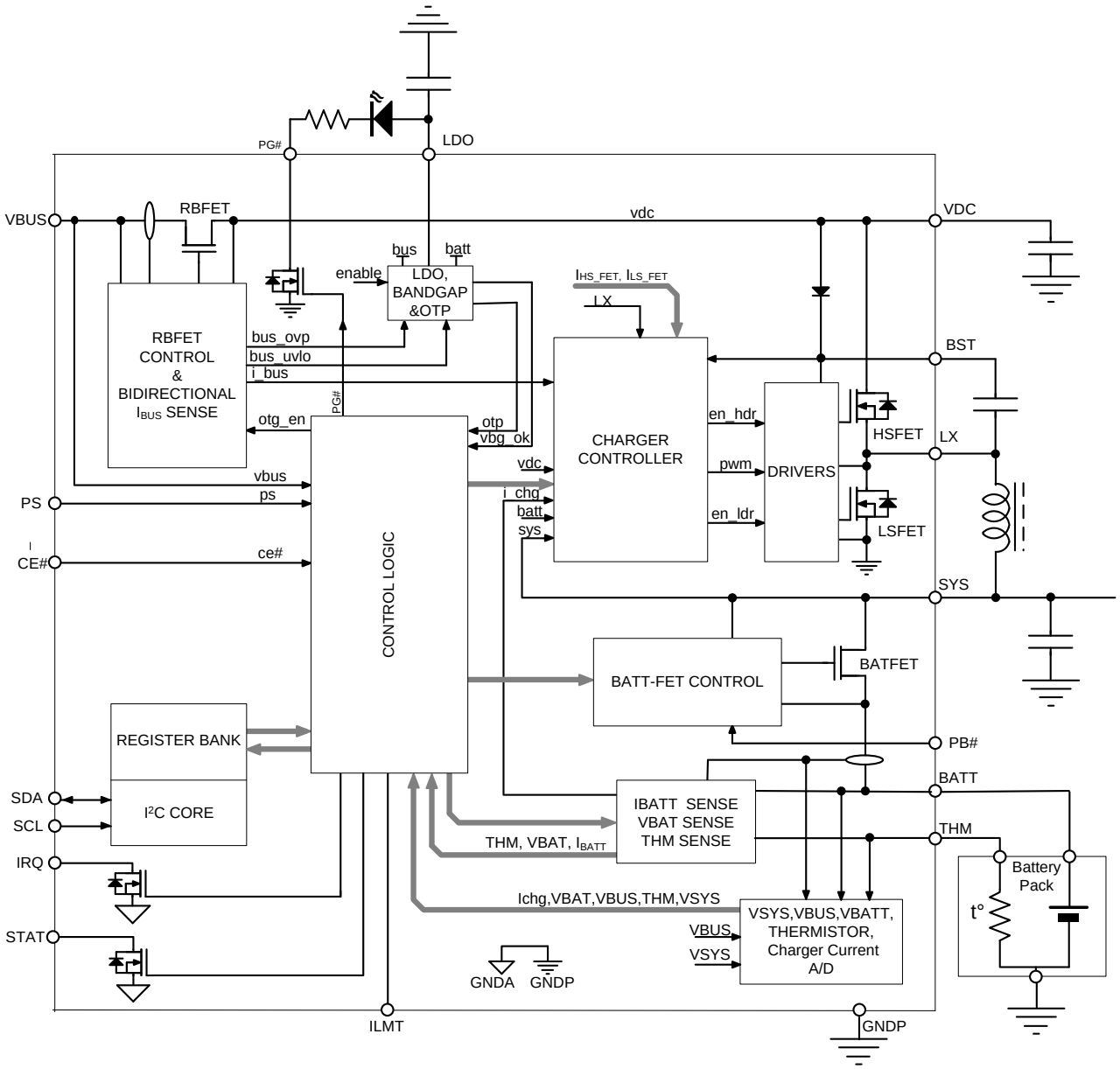

Figure 1: OZ1C82 Block Diagram

PIN DESCRIPTION

Pin	Name	I/O	Type	Description
1	VBUS	P	Power	Solar Panel or USB, adapter input, a 1uF ceramic capacitor should be placed from VBUS to PGND as close as to the IC.
2	PS	I	Digital	Selects default I_{BUS} limit when BUS power becomes available; High indicates a USB source and low indicates an adapter source
3	PG#	O	Digital	Open drain active low power good indicator Connect to the pull-up rail through a 10k resistor
4	STAT	O	Digital	Open drain output signalizing charging status with a 10kΩ pull up resistor: - charging - consistently low - charging legally stopped or charger disabled- consistently high - charging stopped by any fault condition – blinking with 1Hz
5	SCL	I	Digital	Serial I^2C Clock signal; connect by a resistor to pull-up rail.
6	SDA	I/O	Digital	Serial I^2C Data signal; connect by a resistor to pull-up rail.
7	IRQ	O	Digital	Interrupt request output pin – open drain and low pulse active Connect to the pull-up rail through a 10k resistor
8	OTG	I	Digital	Connected to ground.
9	CE#	I	Digital	Charge Enable pin. Active low
10	ILMT	I	Analog	Connected to ground.
11	THM	I	Analog	Input of battery temperature detection circuitry. Connect a NTC resistor to this pin. Program temperature with a resistor divider from LDO to THM to ground. When THM is out of range, charge suspends.
12	PB#	I	Digital	BATFET ON/OFF control pin. When PB# is pull low for $t_{SHIPMODE}$ to turn on BATFET when BATFET is off in shipping mode. When PB# is pull low for t_{PB_RST}(15s typical) without VBUS plugging in, BATFET will turn off then on to reset system.
13	VBAT	P	Power	Battery charger output and battery voltage sense pin. Connect to battery cell. The internal BATFET is connected between VBAT and VSYS, connect a 10uF capacitor closely to VBAT pin
14	VBAT	P	Power	
15	VSYS	P	Power	System voltage output. Connect a 20uF capacitor closely to VSYS pin
16	VSYS	P	Power	
17	GNDP	P	Power	Ground for Power section
18	GNDP	P	Power	
19	LX	P	Power	Switching Node Connection
20	LX	P	Power	
21	BST	P	Power	Positive supply for the high side driver. A 0.047µF capacitor should be placed between BST and LX.
22	LDO	P	Power	Power supply for the internal analog circuit. Bypass to ground by 4.7µF ceramic capacitor placed as close as possible to the pins
23	VDC	P	Power	Charger input node. A 10µF capacitor is needed from this pin to GNDP.
24	NC	-	-	NC

ABSOLUTE MAXIMUM RATINGS

VBUS, VDC to GNDP ..... -0.3V to +18V
LDO, VSYS, VBAT to GNDP ..... -0.3V to +7V
LX referred to GNDP and VDC ..... GNDP-0.5V to VDC+0.5V
PS, STAT, PG#, CE#, PB#, THM, IRQ, ILMT to GNDP ..... -0.3V to LDO+0.3V
BST referred to LX ..... -0.3V to +7V
SCL, SDA to GNDP ..... -0.5V to +7V
Maximum Operating Junction temperature ..... +125°C
Storage temperature range ..... -55°C to +150°C

NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

VBUS, VDC to GNDP ..... 3.9V to 14V
SDA, SCL, PS, STAT, PG#, CE#, PB#, THM, IRQ, ILMT ..... 0V to LDO
VSYS, VBAT ..... 0V to LDO
Operating temperature range (ambient) ..... -40°C to 85°C

ELECTRICAL CHARACTERISTICS

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} > V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST	MIN	TYP	MAX	UNITS
QUIESCENT CURRENTS						
I_{VBUS}	Input supply current (VBUS)	V_{VBUS} = 5 V, High-Z mode, no battery, battery monitor disabled		15	30	µA
		V_{VBUS} = 12V, High-Z mode, no battery, battery monitor disabled		30	50	µA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter not switching		1.5	3	mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT}=3.2V, I_{SYS}=0A		3		mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT}=3.8V, I_{SYS}=0A		3		mA
VBUS/BAT POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		14	V
V_{VBUS_UVLOZ}	VBUS for active I^2C, no battery	V_{VBUS} rising	3.6			V
V_{SLEEP_F}	Sleep mode falling threshold	V_{VBUS} falling, $V_{VBUS-VBAT}$	25	65	120	mV
V_{SLEEP_R}	Sleep mode rising threshold	V_{VBUS} rising, $V_{VBUS-VBAT}$	130	250	370	mV
V_{ACOV}	VBUS over-voltage rising threshold	V_{VBUS} rising	14		15	V
	VBUS over-voltage falling threshold	V_{VBUS} falling	13.5		14.5	
V_{BAT_UVLOZ}	Battery for active I^2C, no VBUS	V_{BAT} rising	2.3			V

ELECTRICAL CHARACTERISTICS (Continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} > V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ON(HSFET)}$	Internal top switching MOSFET on resistance between VDC and LX	T_J = –40°C – 85°C		22		mΩ
		T_J = -40°C – 125°C		22		
$R_{ON(LSFET)}$	Internal bottom switching MOSFET on-resistance between LX and PGND	T_J = –40°C – 85°C		24		mΩ
		T_J = -40°C – 125°C		24		
V_{FWD}	BATFET forward voltage in supplement mode	Battery discharge current 10mA		30		mV
BATTERY CHARGER						
V_{BAT_RANGE}	Typical charge voltage range	V_{BAT}	3.84		4.608	V
V_{BATRG_STEP}	Typical charge voltage step			16		mV
$V_{BAT\_REG\_ACC}$	Charge voltage regulation accuracy	V_{BAT} = 4.208V or 4.352V	–0.5		0.5	%
$I_{CHG\_REG\_RANGE}$	Typical fast charge current regulation range	I_{CHG}	0		3000	mA
$I_{CHG\_REG\_STEP}$	Typical fast charge current regulation step			64		mA
$I_{ICHG\_REG\_ACC}$	Fast charge current regulation accuracy	V_{BAT} =3.8V, I_{CHG} = 128mA T_J = -40°C-85°C	–20		20	%
		V_{BAT} =3.8V, I_{CHG} = 256mA T_J = –40°C – 85°C	–10		10	
		V_{BAT} = 3.8V, I_{CHG} = 1792mA T_J = –40°C – 85°C	–5		5	
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, REG06[1] = 1	2.6	2.8	2.9	V
	Battery LOWV rising threshold	Precharge to fast charge, REG06[1] = 0	2.8	3.0	3.1	V
I_{PRECHG_RANGE}	Precharge current range	I_{PRECHG}	64		1024	mA
I_{PRECHG_STEP}	Typical precharge current step	I_{PRECHG_STEP}		64		mA
I_{TERM_RANGE}	Termination current range	I_{TERM_RANGE}	64		1024	mA
I_{TERM_STEP}	Termination current step	I_{TERM_STEP}		64		mA
$V_{BATSHORT}$	Battery Short Voltage	V_{BAT} falling		2		V
$V_{BATSHORT\_HYST}$	Battery Short Voltage hysteresis	V_{BAT} rising		200		mV
I_{SHORT}	Battery short current (trickle current)	V_{BAT}<2.2V		100		mA
V_{RECHG}	Recharge threshold below V_{BATREG}	V_{BAT} falling, REG06[0] = 0		100		mV
		V_{BAT} falling, REG06[0]=1		200		mV
$R_{ON(BATFET)}$	SYS-BAT MOSFET on-resistance	T_J = 25°C		12		mΩ
$I_{BATLOAD}$	Battery discharge load current	V_{BAT}=4.2V		15		mA
$I_{SYSLOAD}$	System discharge load current	V_{SYS}=4.2V		30		mA
Input Voltage/Current Regulation						
V_{INDPM_RANGE}	Typical input voltage range	V_{BUS}	3.9		15.3	V
V_{INDPM_STEP}	Typical input voltage regulation step	V_{VBUS_STEP}		100		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM=4.4V	–3		3	%
I_{INDPM_RANGE}	Typical input current range	ILMTSET	100		2400	mA
I_{INDPM_STEP}	Input current regulation step	ILMTSET_STEP	50			mA
I_{INDPM_ACC}	Input current regulation accuracy, V_{BAT}=5V, current pulled from LX	USB500,ILIMSET(REG00[5:0])=500mA	440		500	mA
		Adapter 1.5A, ILIMSET(REG00[5:0])=1500mA	1300		1500	mA
K_{ILIM}	$I_{INMAX}=K_{ILIM}/R_{ILIM}$	Input current regulation by ILIM pin=1.5A	320		390	AxΩ

OZ1C82 DS

ELECTRICAL CHARACTERISTICS (Continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} > V_{SLEEP}$, T_J = –40°C to +125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic I/O pin Characteristics (CE#,PS,PB#)						
V_{IH}	Input high threshold level		1.3			V
V_{IL}	Input low threshold level				0.4	V
I_{IN_BIAS}	High level leakage current	Pull-up rail 1.8V			1	uA
$V_{PB\#}$	Inter PB# pull-up	Battery only mode		VBAT		V
		V_{VBUS}=9V		5.1		
		V_{VBUS}=5V		4.8		
$R_{PB\#}$	Internal PB# pull-up resistance			1		MΩ
Logic I/O pin Characteristics (IRQ,STAT,PG#)						
V_{OL}	Output low threshold level	Sink current=5mA			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8V			1	uA
I^2C Interface (SCL,SDA)						
V_{IH}	Input high threshold level, SCL and SDA	Pull-up rail 1.8V	1.3			V
V_{IL}	Input low threshold level, SCL and SDA	Pull-up rail 1.8V			0.4	V
V_{OL}	Output low voltage level	Sink current=5mA			0.4	V
I_{BIAS}	High level leakage current	Pull-up rail 1.8V			1	uA

Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I^2C Interface (SCL,SDA)						
f_{SCL}	SCL clock frequency				400[Note 1]	kHz
Battery Over-voltage Protection						
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		us
Battery Charger						
t_{RECHG}	Recharge deglitch time			20[Note 1]		ms
Battery monitor						
t_{CONV}	Conversion time	CONV_RATE(REG02[6])=1			1000[Note 1]	ms
PB# and Shipping Timing						
$t_{SHIPMODE}$	PB# low time to turn on BATFET and exit ship mode	T_J=-10°C-60°C		1.75[Note 1]		sec
t_{QON_RST}	PB# low time to enable full system reset	T_J=-10°C-60°C		15[Note 1]		sec
t_{BATFET_RST}	BATFET off time during full system reset	T_J=-10°C-60°C		450[Note 1]		ms
t_{SM_DLY}	Enter ship mode delay	T_J=-10°C-60°C		12.5[Note 1]		sec
Digital Clock and Watchdog Timer						
f_{LPDIG}	Digital low power clock	LDO disabled		30		kHz
f_{DIG}	Digital clock	LDO enabled		1000		kHz
t_{WDT}	Watchdog time	Watchdog (REG07[5:4]=01),LDO enabled		40[Note 1]		sec

Note 1: all the items with Note 1

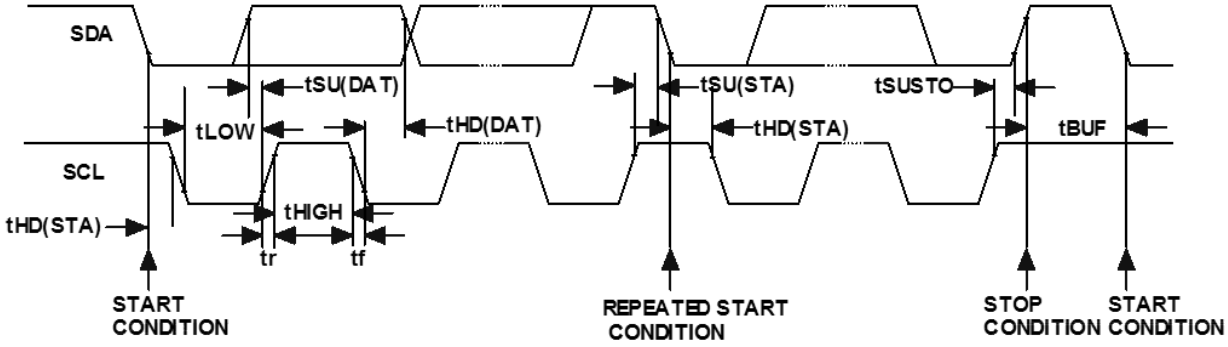

Figure 2 :I^2C Timing Diagram

FUNCTIONAL DESCRIPTION

Device power-on-reset (POR)

The internal bias circuit is powered from the higher voltage between VBUS and VBAT. When VBUS rises above V_{VBUS_UVLOZ} or VBAT rises above V_{VBAT_UVLOZ}, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all registers are reset to default value. The host can access all the registers after POR.

Device powered up from battery without input source

When only battery is present and the battery voltage is above the depletion threshold (V_{BAT_DPLZ}), the BATFET turns on and connects battery to system. The LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and low quiescent current on VBAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharging current through BATFET.

When the system is overloaded or shorted($I_{BAT}>I_{BATFET\_OCP}$), the device turns off BATFET immediately and sets BATFET_DIS bit to indicate BATFET is disabled until input source is plugged in again or BATFET is re-enabled again.

Device powered up from input source

When an input source is plugged in, the device checks the input source voltage to turn on LDO and all the bias circuit. It detects and sets the input current limit before the buck converter is started when AUTO_DPDM_EN bit is set. The power up sequence from input source is as listed:

1. Power up LDO
2. Input source type detection based on PS to set the default input current limit register and input source type.
3. Input voltage limit threshold setting
4. Converter power up

Power up LDO regulation

LDO supplies the internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to THM external resistors. The pull-up rail of STAT and PG# can be connected to LDO as well. The LDO is enabled when all the below conditions are valid:

1. VBUS above the V_{VBUS_UVLOZ}
2. VBUS above $V_{BAT}+V_{SLEEPZ}$ in buck mode
3. After 220ms delay is completed

If one of the above conditions is not valid, the device is in high impedance mode (**HIZ**) with LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during **HIZ** state. The battery powers up the system when device is in **HIZ**.

Poor Power Qualification

After LDO powers up, the input source has to meet the following requirements in order to start the buck converter.

1. BUS voltage below V_{ACOV}
2. VBUS voltage above $V_{VBUSMIN}$

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and IRQ pin sends a pulse to the host, if the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

Input current limit detection and input current limit setting

OZ1C82 runs VBUS input current limit detection by PS pin after VBUS is plugged in and LDO powers up, and then sets VBUS input current limit default value into IINLIM register that can be read by host as below:

Table 1: IINLIMIT detection

Input detection	PS	IINLIM (mA)	0x0Bh bit[7:5]
USB SDP (USB500)	High	500	001
Adapter	Low	3250	010

Anytime, host can set IINLIM register 0x00h by I^2C. The charger input current is always limited by the lower of IINLIM or ILIM pin.

Input voltage limit detection and input voltage limit setting (VINDPM Threshold)

OZ1C82 supports wide range of input voltage limit (3.9V-14V) for high voltage charging and provides two methods to set input voltage limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM
   By setting FORCE_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writeable and allows host to set the absolute threshold of VINDPM function.
2. Relative VINDPM
   When FORCE_VINDPM bit is 0(default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM threshold setting algorithm. The algorithm allows a wide range of adapter (V_{VBUS_OP}) to be used with flexible VINDPM threshold.

Converter power up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If the battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rails ramp up. When the system rail is below 2.2V, the input current limit is

forced to the lower of 100mA or ILIM pin. After the system rises above 2.2V, the device limits the input current to the lower value of ILIM pin and IINLIM register.
In order to improve the light–load efficiency, the device enters skip mode at light load.

Input current optimizer (ICO)

OZ1C82 provides input current optimizer (ICO) to indentify maximum power point without overload the input source. The algorithm automatically identifies maximum input current limit of power source without entering VINDPM to avoid input source overload.

The feature is disabled by default (ICO_EN=0) and can be enabled by setting ICO_EN bit to 1. After the input source is detected, ICO runs automatically when ICO_EN bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type 794(w)1.064 Tm[( )] TJETBT1 0 051 250.37 499.2i Tm[(l-5(i)-4(n)] TJETBT1 0 051 250.37 4

For safe operation, the host should set the maximum allowed regulation voltage register and the minimum resistance compensation.

JEITA guideline compliance in charge mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charging current and high charging voltage at certain low and high temperature ranges.

The OZ1C82 continuously monitors battery temperature by measuring the voltage between the THM pin and ground, typically determined by a negative temperature coefficient thermistor (NTC) and an external voltage divider. The OZ1C82 compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle; the voltage on THM pin must be within the VT1 to VT5 thresholds. If THM voltage exceeds the T1–T5 range, the controller suspends charging and the LED connecting to ST pin

1. VBUS source identified (through PS detection and OTG pin)
2. VBUS power source good
3. VBUS above battery (not in sleep)
4. VBUS removed or below V_{ACOV} threshold
5. VBUS above $V_{VBUSMIN}$ (typical 3.8V) (not a poor source)
6. Charge Complete
7. Any fault event in REG0C

When a fault occurs, OZ1C82 sends out IRQ and keeps the fault state in REG0C until the host reads REG0C. Before the host reads REG0C and all the faults are cleared, OZ1C82 wouldn't send any IRQ upon new faults. To read the current fault status, the host has to read REG0C twice consecutively. The 1st read reports the pre-existing fault status and the 2nd read reports the current fault status.

Safety Timer

If the safety timer is expired, the switch between VSYS and VBAT is off to prevent further charging, and LED blinks on and off with 1Hz frequency. The buck converter keeps enabled to supply system. CHRG_FAULT bits set to 11 and IRQ will generate 250µs low pulse. In charging mode, fast charging safety timer is programmed by REG07 [2:1], wake up timer is default 4hours. The safety timer can be disabled by setting EN_TIMER=0

During input voltage, current or thermal regulation, the safety timer counts at half clock rate because the real charge current could be lower than the register setting. This half clock rate feature can be disabled by setting EN_TMR2X=0

VBUS OVP (ACOV)

When VBUS voltage exceeds V_{ACOV}, OZ1C82 will stop switching immediately. During ACOV, the fault register CHRG_FAULT bits set to 01 and an IRQ asserts to the host.

System OVP

When over voltage happens for system, both buck converter and BATFET between VSYS and VBAT are off. The charging will be automatically restarted when OVP condition disappears.

System OCP

When the system is shorted or significantly overloaded ($I_{BAT}>I_{BATOP}$) so that its current exceeds the over-current limit, OZ1C82 latches off BATFET. BATFET Enable Section (Exit shipping mode) can reset the latch-off condition and turn on BATFET.

Thermal Protection in Buck Mode

OZ1C82 monitors the internal junction temperature T_J to avoid overheat and limits IC surface temperature in buck mode. When T_J exceeds the preset thermal regulation limit by TREG bits (REG08[1:0]), the charge current would be lowered down. During thermal regulation, the actual charging current is usually below the setting charging current. So termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

OZ1C82 has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT}. The fault register CHRG_FAULT is set to 10 and IRQ is asserted to the host. The converter and BATFET will be enabled to recover when IC temperature lower than T_{SHUT_HYST}.

Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charging function is disabled immediately. And the fault register BAT_FAULT bit goes high.

Battery Over-Discharge Protection

When battery is discharged below V_{BAT_DPL}, BATFET will be turned off to protect battery from over discharge. Battery will recover to be normal when an input source detected at VBUS. When an input source is plugged in, BATFET turns on, and the battery is charged with I_{SHORT} (typical 100mA) current when $V_{BAT}<V_{BATSHORT,}$ or pre-charge current as set in IPRECHG register when the battery voltage is between $V_{BATSHORT}$ and $V_{BATLOWV}$.

Battery Monitor

OZ1C82 can report V_{VBUS}, V_{BAT}, V_{SYS}, thermistor ratio, and charging current in battery monitor registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by CONV_RATE bit (REG02[6]): one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV_RATE=0), the CONV_START bit needs to be set 1 to start the conversion. And CONV_START bit is cleared by OZ1C82 when conversion is completed. The conversion result is ready after t_{CONV} (maximum 1 second)

For continuous conversion (CONV_MODE=1), the CONV_START needs to be set 1 to start the conversion. During active conversion, the CONV_START keeps 1 to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV_START is cleared.

BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, OZ1C82 can turn off BATFET by setting BATFET_DIS=1

so that the system voltage is zero to minimize the battery leakage current. And BATFET can turn off immediately or delay by t_{SM_DLY} as defined by BATFET_DLY bit.

BATFET Enable (Exit Shipping Mode)

BATFET can be enabled to restore system power by one of the following events:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST=1 to reset all the registers including BATFET_DIS bit to default 0
4. A logic high to low transition on PB# with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit shipping mode

Standby Mode Charge

In standby mode, there is no I^2C command to be sent by host when both VBUS and battery are active, PS and CE# are low active; in this case, OZ1C82 can also complete a charging cycle automatically with default charging parameters are listed in the following table.

Table 3: Default charger parameters

Standby mode	**Default charging parameters**
Charging Voltage	4.208V
Charging Current	2048A
Wake up Current	128mA
Termination current	256mA
Recharging threshold	100mV
Wake up timer	4 hours
CC Charge timer	12 hours
Wake up threshold	3V
V_{SYSMIN} threshold	3.5V

Anytime, host can access OZ1C82 and change the charger parameters by I^2C according to customer's charging requirements

Constant Voltage and Constant Current Operation

As shown in Figure 5, the charger in OZ1C82 uses six error amplifiers: EA1 for the adapter current limitation, EA2 for charging voltage regulation, EA3 for charging current regulation, and EA4 for VBUS voltage regulation, EA5 for system voltage regulation, and EA6 for thermal regulation. The outputs of these four error amplifiers are tied to the COMP pin for compensation.

The output of the adapter current-sense amplifier is connected to the error amplifier EA1. EA1's output is connected to the COMP pin. Therefore, whenever the AC adapter current limit is exceeded, EA1 output will control the COMP voltage. The charger's duty cycle will be reduced until the total adapter current falls within its limit value.

In a constant current regulation operation, the error amplifier EA3 will control the COMP pin voltage. The circuit operates to regulate the charger output current according to the desired current setting by I^2C programming with ±5% accuracy.

In a constant voltage operation, the error amplifier, EA2 will control the COMP pin. The circuit operates to regulate the charger output voltage according to the desired voltage setting by I^2C programming with ±0.5% accuracy.

In a VBUS voltage regulation operation, the error amplifier, EA4 will control the COMP pin. The circuit operates to regulate the VBUS input voltage according to the VBUS VLMT voltage setting by I^2C programming with ±3% accuracy.

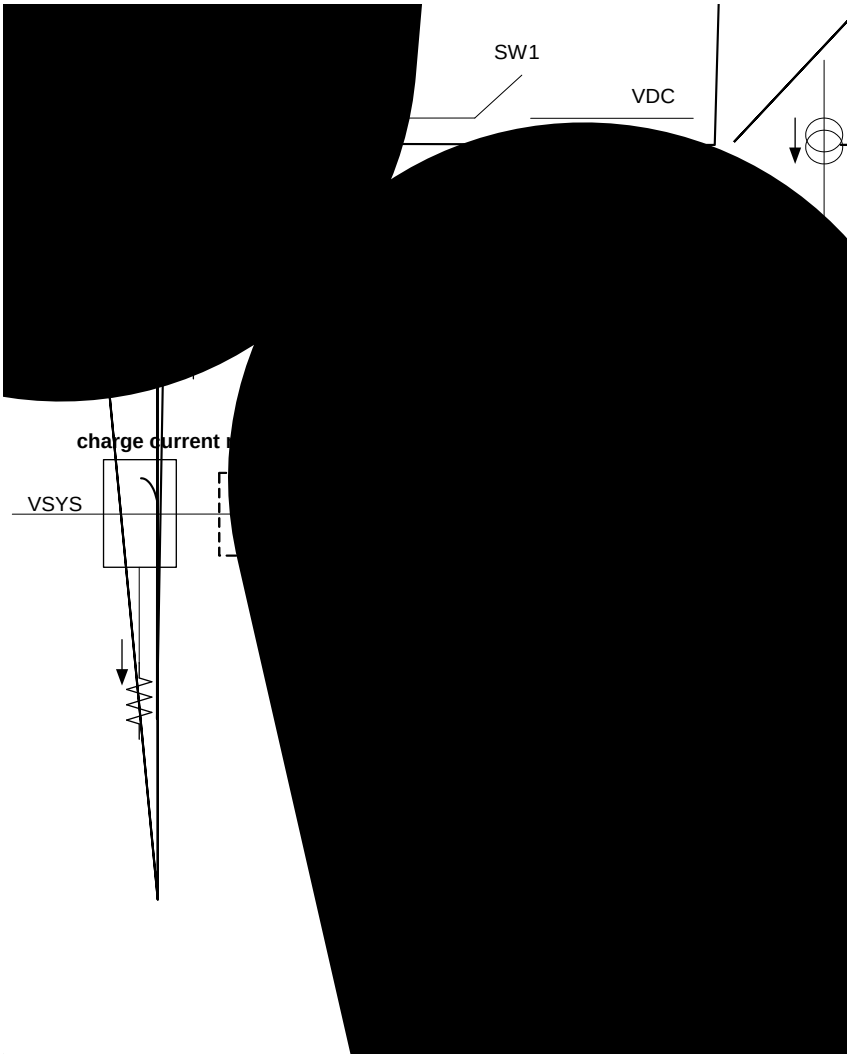

Figure 5: Voltage, Current and Thermal regulation loops

Serial Interface

The device uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

a) Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

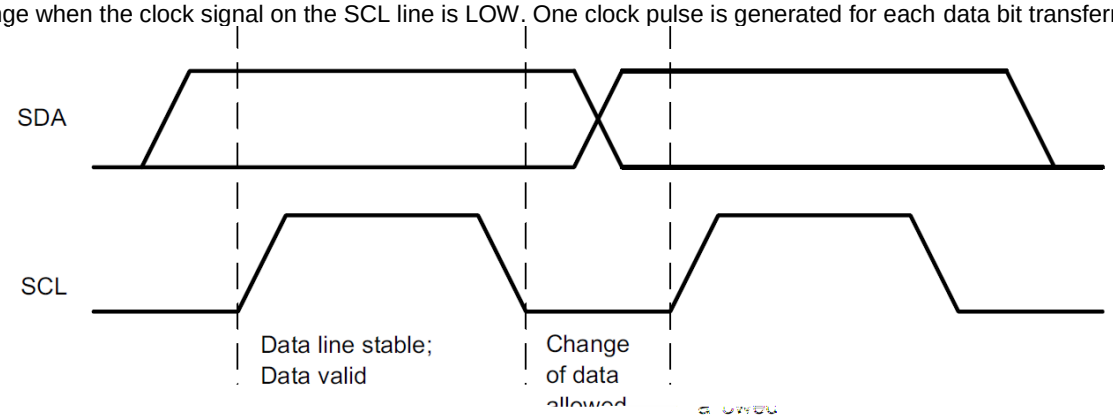

Figure 6: Bit Transfer on the I^2C Bus

b) START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

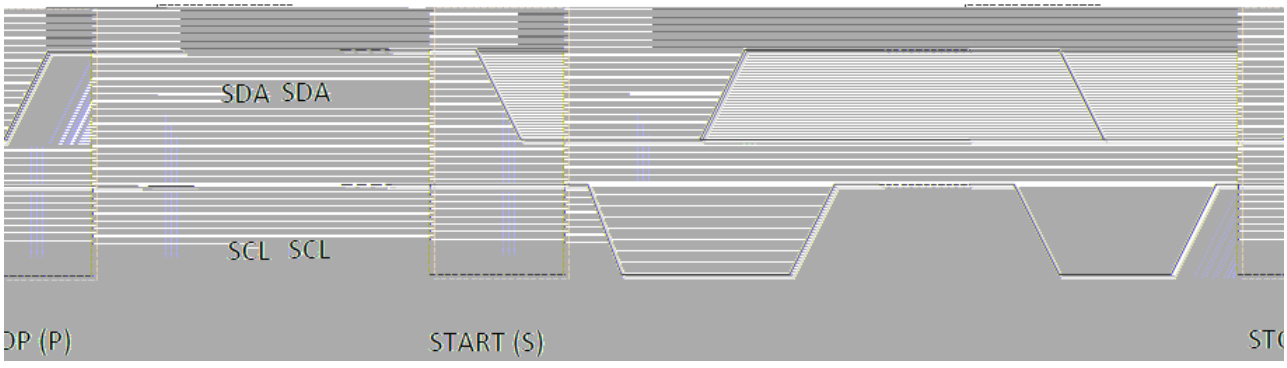

Figure 7: START and STOP conditions

c) Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

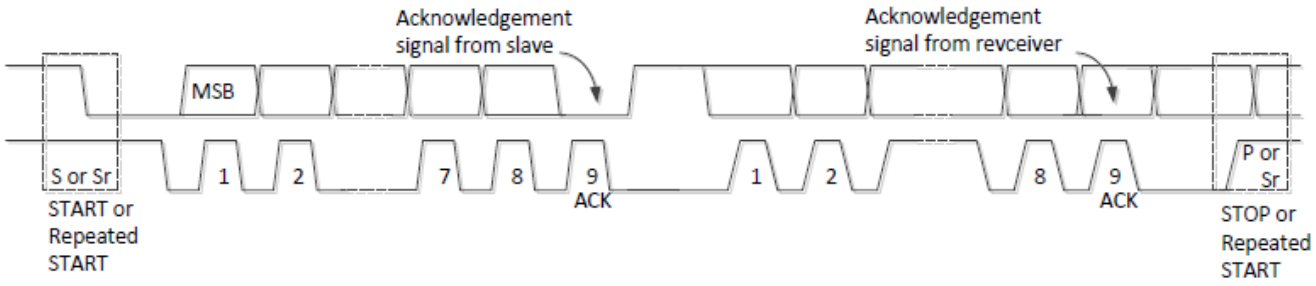

Figure 8: DATA Transfer on the I^2C Bus

d) Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

e) Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

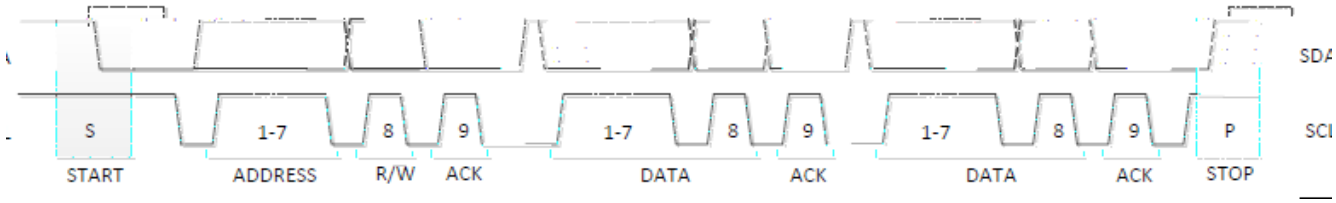

Figure 9: Complete Data Transfer

f) Single Read and Write

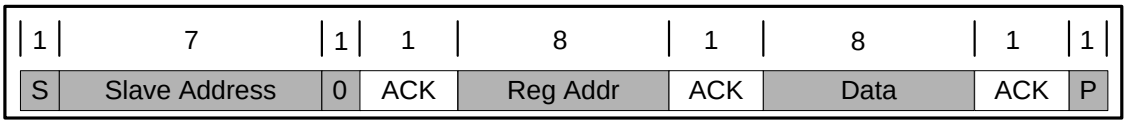

Figure 10: Single Write

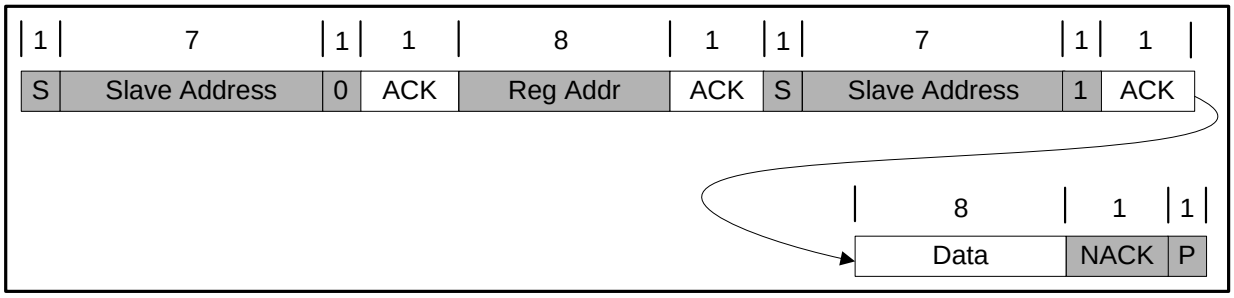

Figure 11: Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

g) Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.

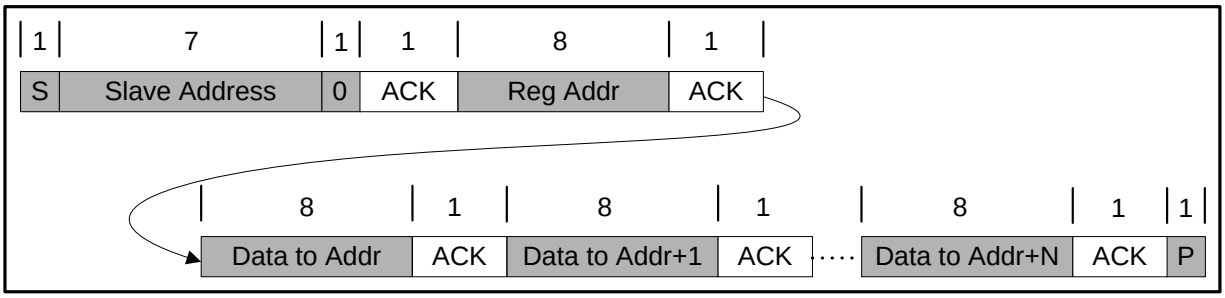

Figure 12: Multi-Write

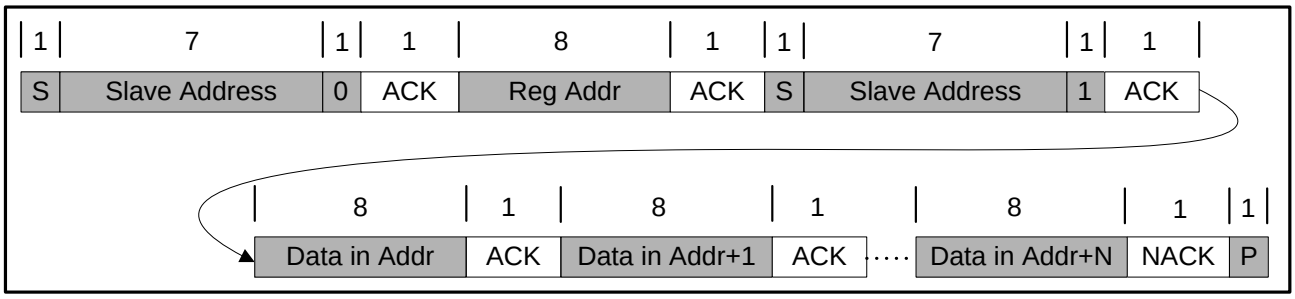

Figure 13: Multi-Read

REG0C is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG0C reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG0C for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REG0C does not support multi-read and multi-write.

Host mode and default mode

The OZ1C82 is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charge is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After POR, the device starts in default mode with watchdog timer expired, or default mode, all the registers are in the default settings.

In default mode, the device keeps charging the battery with 12-hour fast charging safety timer. At the end of 12 hour, the charging is stopped and the buck converter continues to operate to supply system load. Any write command to the device will switch the default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WATCHDOG_RST bit before watchdog timer expires(WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG_FAULT bit=1) is expired, the device returns to default mode and all registers are reset to default value except IINLIM, VINDPM_OS, BATFET_RST_EN, BATFET_DLY and BATFET_DIS bits.

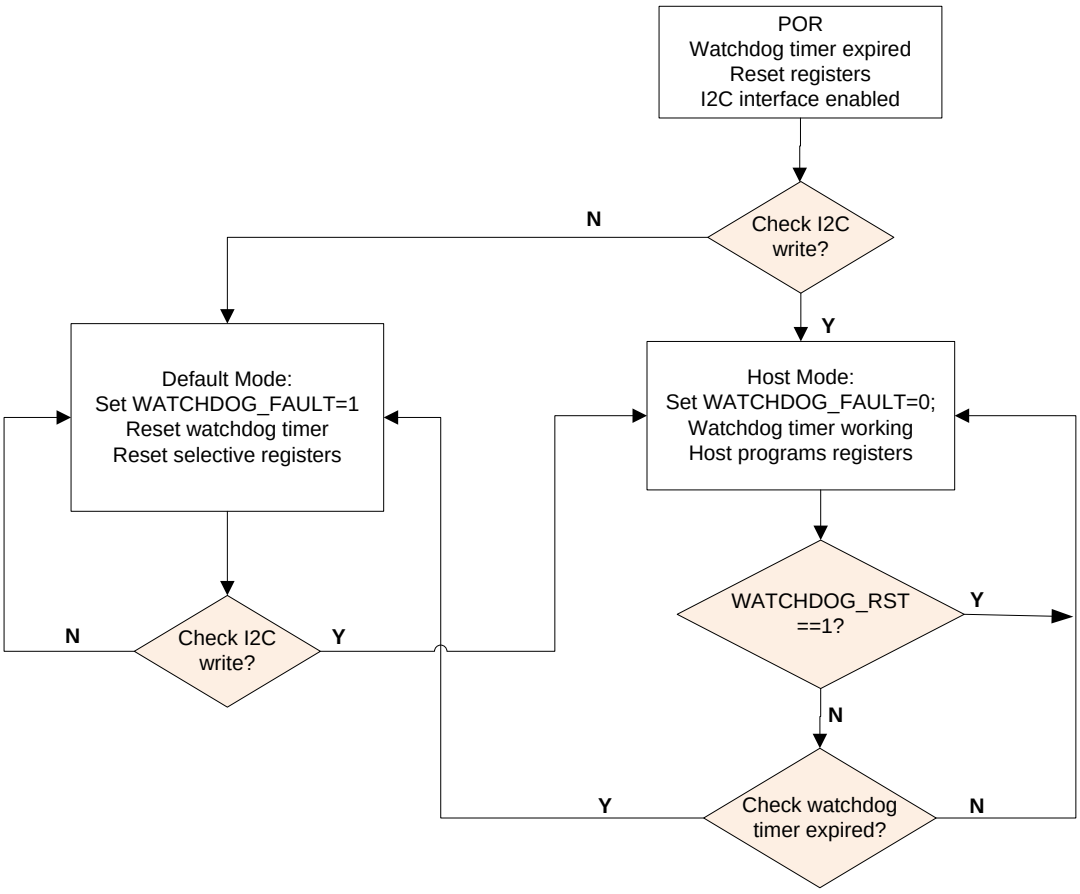

Figure 14: Watchdog timer for host mode and default mode

REGISTER MAP

Register index (hex)	Bit Number							
	EN_HIZ	EN_ILIM	IINLIM[5:0]					
	Reserved	Reserved	Reserved	VINDPM_OS[4:0]				
	CONV_START	CONV_RATE	Reserved	ICO_EN	Reserved	Reserved	FORCE_DPDM	AUTO_DPDM_EN
	BAT_LOADEN	WD_RST	Reserved	CHG_CONFIG	SYSMIN[2:0]			Reserved
	EN_PUMPX	ICHG[6:0]						
	IPRECHG[3:0]				ITERM[3:0]			
	VREG[5:0]						BATLOWV	VRECHG
	EN_TERM	Reserved	WATCHDOG[1:0]		EN_TIMER	CHG_TIMER[1:0]		JEITA_ISET (0°C-10°C)
	BAT_COMP[2:0]			VCLAMP[2:0]			TREG[1:0]	
	FORCE_ICO	TMR2X_EN	BATFET_DIS	JEITA_VSET (45°C-60°C)	BATFET_DLY	BATFET_RST_EN	PUMPX_UP	PUMPX_DN
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	VBUS_STAT[2:0]			CHRG_STAT		PG_STAT	Reserved	VSYS_STAT
	WATCHDOG_ FAULT	Reserved	CHRG_FAULT		BAT_FAULT	NTC_FAULT[2:0]		
	FORCE_VINDPM	VINDPM[6:0]						
	THERM_STAT	BATV[6:0]						
	Reserved	SYSV[6:0]						
	Reserved	TSPCT[6:0]						
	VBUS_GD	VBUSV[6:0]						

DETAILED REGISTER INFORMATION

This part describes the register definition and configuration for OZ1C82.
The following describes the register definition and configuration for charger module. Its I²C slave write address is **D6H** and the slave read address is **D7H**.

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■ TYPICAL APPLICATION SCHEMTAIC

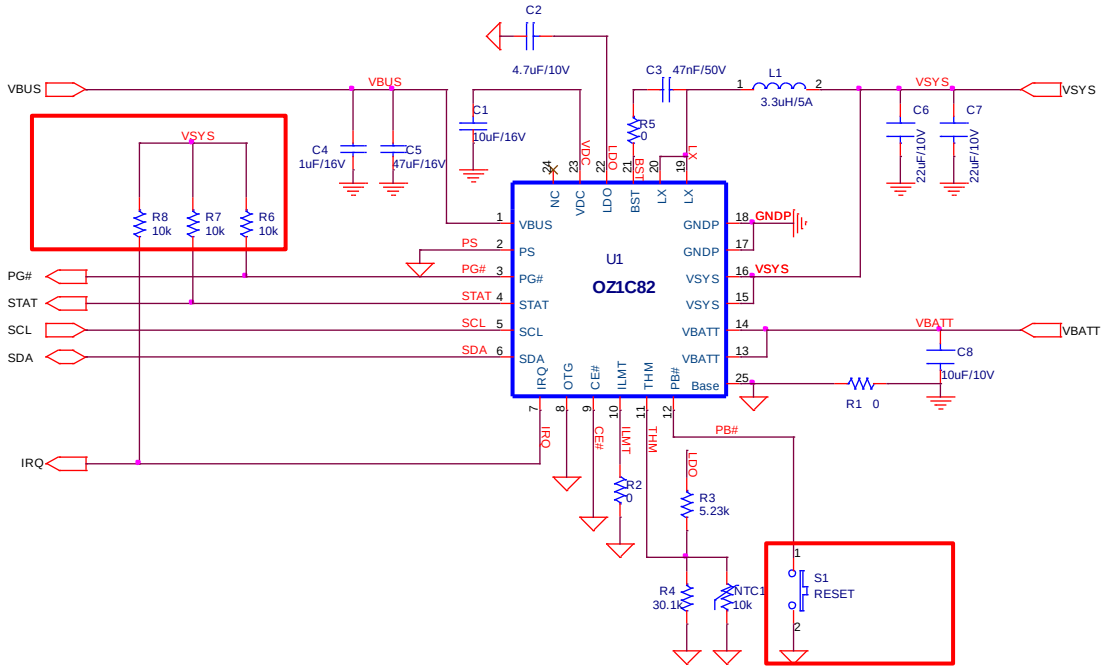

Figure 15: OZ1C82 Typical Application Schematic

BILL OF MATERIALS

Item	Qty	Reference	Value	Vendor	Part Number	PCB Footprint
1	1	C1	10μF/16V	Any	Ceramic – X7R or X5R	0805
2	1	C2	4.7μF/10V	Any	Ceramic – X7R or X5R	0805
3	1	C3	47nF/50V	Any	Ceramic – X7R or X5R	0603
4	1	C4	1μF/16V	Any	Ceramic – X7R or X5R	0603
5	1	C5	47μF/16V	Any	Ceramic – X7R or X5R	0805
6	2	C6,C7	22μF/10V	Any	Ceramic – X7R or X5R	0805
7	1	C8	10μF/10V	Any	Ceramic – X7R or X5R	0805
8	2	R1,R2	0Ω	Any	-	0603
9	1	R3	5.23kΩ 1%	Any	-	0603
10	1	R4	30.1kΩ1%	Any	-	0603
11	1	R5	0Ω	Any	-	0603
12	3	R6,R7,R8	10kΩ	Any	-	0603
13	1	NTC	103AT	-	-	0603
14	1	L1	3.3μH/5A	Würth Elektronik	74437346033	7.3x6.6x2.8
15	1	U1	-	O2Micro, Inc.	OZ1C82	QFN24 4mmx4mm

COMPONENT SUPPLIERS

Manufacturer	Contact Information	
	Phone	Website
Inductors		
Würth Elektronik	+49 (0) 79 42 945 -5000	http://www.we-online.com
Capacitors		
Vishay	1-847-803-6100	www.vishay.com
Johanson Dielectrics	1-818-364-9800	www.johansondielectrics.com
TDK	1-800-344-2112	www.tdk.com
SANYO	N/A	http://www.sanyo.com/components/
Würth Elektronik	+49 (0) 79 42 945 -5000	http://www.we-online.com
Resistors		
Vishay	1-402-563-6866	www.vishay.com
TDK	1-800-344-2112	www.tdk.com

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