

Preliminary OZ1C82 DS

## **Change Summary**

## CHANGES

No.	Applicable Section	Description	Page(s)
1	Electrical Characteristic	Updated	5-8
2	General description	Updated	2
3	Functional description	Updated	10,11,13,15
4	Typical application schematic	Updated	28
5			
6			
7			
8			

## **REVISION HISTORY**

Revision No.	Description of change Relea	
0.5	Initial release	2017/12/05
0.7	Updated #1	2018/03/12
0.71	The changes are listed above from #2 to #3,#4	2018/05/09



## I<sup>2</sup>C Controlled 3A Fully Integrated 1 Cell Li-Ion Battery NVDC Charger with MPPT control for Solar Panel

### FEATURES

- High accuracy switched mode 1 cell Li-lon charger with integrated synchronous switching MOSFETs
- Support Intel NVDC topology
- Support Quick Charge, VBUS input voltage up to 14V
- Support VINDPM mode to set the MPPT voltage using for solar panel power
- Input current optimization function to identify the maximum input power to not overload
- Dynamically allocates USB input power including input voltage regulation and input current limit to adapt all kinds of adapter
- Constant ripple current (CRC) control and no external loop compensation
- Integrated charging sensing resistor and input current sensing resistor
- Integrated bootstrap diode
- Support USB 2.0, 3.0 USB Standards and higher voltage adapter
- Setting charging current from 0A to 3A
- Integrated 15mΩ battery discharge MOSFET up to 9A pulse discharge current to get highest battery discharging efficiency
- I<sup>2</sup>C programmable battery path impedance compensation to accelerate charge time
- Up 93% charge efficiency at 2A and 91% at 3A
- I<sup>2</sup>C setting and battery charge management
  - ±0.5% voltage mode accuracy
    - ±5% current mode accuracy
  - ±3% VBUS input voltage limit accuracy
- 100mA to 3.25A input current limit
- VBUS UVLO and Over-Voltage Protection, VSYS
   Over-Voltage Protection
- Power MOSFETs Over-Current Protection
- Support shipping mode
- Joint Power Supply when system over load
- Support autonomous battery charging process without I<sup>2</sup>C communication
- Provides telemetry and charging status indication information via I<sup>2</sup>C(voltage, temperature, current)
- Interrupt output IRQ to host
- Thermal regulation and Over Temperature Protection
- Charger safety timer
- Low battery current dissipation when only battery present
- Lead free and RoHS Compliant

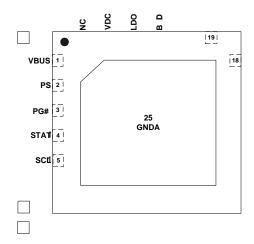
#### APPLICATIONS

- Shared bike
- Cell Phone
- Other Solar Panel devices

# ORDERING INFORMATION Part Number | Temp Range |

<b>OZ1C82</b> -40	°C to 125°C	QFN24, 4mmx4mm

### **PIN DIAGRAM**







### GENERAL DESCRIPTION

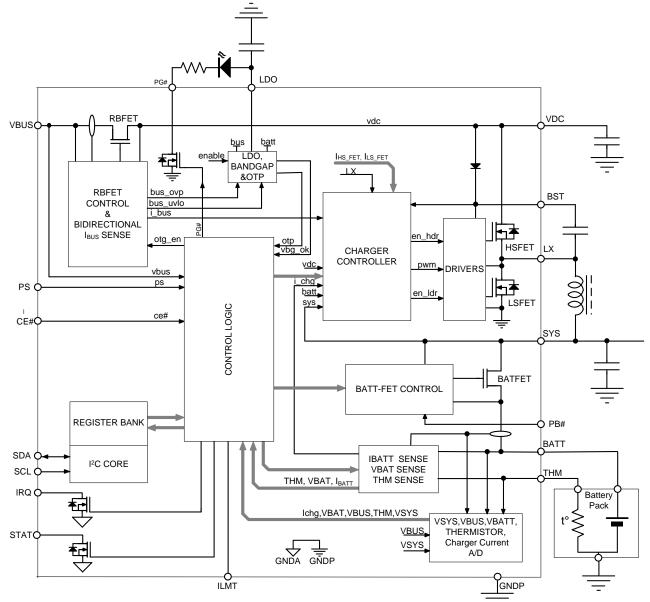
OZ1C82 is an I<sup>2</sup>C controlled power management IC for single cell Lilon or Li-polymer battery systems in a wide input range of Solar panel powered devices, like shared bike, power bank or other portable device.

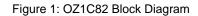
# OZ1C82nstapports allokinals mail 3nput csoz4ces (nha(h)pt age on 4 Tm-3 (3880F2 9 Tf1 0 0 1 121.58 668.62 Tm341.47E63 ()-1TJETro)7(I)-4(I)-range is from 3.9V up to 14V in operation, which is very suitable for solar panel application since the solar panel

voltage is variable with different weather ere



### **BLOCK DIAGRAM**







## **PIN DESCRIPTION**

Pin	Name	I/O	Туре	Description
1	VBUS	Р	Power	Solar Panel or USB, adapter input, a 1uF ceramic capacitor should be placed from VBUS to PGND as close as to the IC.
2	PS	I	Digital	Selects default I <sub>BUS</sub> limit when BUS power becomes available; High indicates a USB source and low indicates an adapter source
3	PG#	0	Digital	Open drain active low power good indicator Connect to the pull-up rail through a 10k resistor
4	STAT	0	Digital	Open drain output signalizing charging status with a 10kΩ pull up resistor: - charging - consistently low - charging legally stopped or charger disabled- consistently high - charging stopped by any fault condition – blinking with 1Hz
5	SCL		Digital	Serial I <sup>2</sup> C Clock signal; connect by a resistor to pull-up rail.
6	SDA	I/O	Digital	Serial I <sup>2</sup> C Data signal; connect by a resistor to pull-up rail.
7	IRQ	0	Digital	Interrupt request output pin – open drain and low pulse active Connect to the pull-up rail through a 10k resistor
8	OTG		Digital	Connected to ground.
9	CE#	I	Digital	Charge Enable pin. Active low
10	ILMT		Analog	Connected to ground.
11	ТНМ	I	Analog	Input of battery temperature detection circuitry. Connect a NTC resistor to this pin. Program temperature with a resistor divider from LDO to THM to ground. When THM is out of range, charge suspends.
12	PB#	I	Digital	BATFET ON/OFF control pin. When PB# is pull low for t <sub>SHIPMODE</sub> to turn on BATFET when BATFET is off in shipping mode. When PB# is pull low for t <sub>PB_RST</sub> (15s typical) without VBUS plugging in, BATFET will turn off then on to reset system.
13	VBAT	Р	Power	Battery charger output and battery voltage sense pin. Connect to battery cell. The internal BATFET is connected between VBAT
14	VBAT	Р	Power	and VSYS, connect a 10uF capacitor closely to VBAT pin
15	VSYS	Р	Power	System voltage output.
16	VSYS	Р	Power	Connect a 20uF capacitor closely to VSYS pin
17	GNDP	Р	Power	Ground for Power section
18	GNDP	Р	Power	Ground for Power section
19	LX	Р	Power	Switching Node Connection
20	LX	Р	Power	Switching Node Connection
21	BST	Р	Power	Positive supply for the high side driver. A 0.047µF capacitor should be placed between BST and LX.
				Power supply for the internal analog circuit. Bypass to ground by
22	LDO	Р	Power	$4.7\mu$ F ceramic capacitor placed as close as possible to the pins
22 23	LDO VDC NC	P P	Power Power	4.7 $\mu$ F ceramic capacitor placed as close as possible to the pins Charger input node. A 10 $\mu$ F capacitor is needed from this pin to GNDP.



### **ABSOLUTE MAXIMUM RATINGS**

VBUS, VDC to GNDP	-0.3V to +18V
LDO, VSYS, VBAT to GNDP	
LX referred to GNDP and VDC	GNDP-0.5V to VDC+0.5V
PS, STAT, PG#, CE#, PB#, THM, IRQ, ILMT to GNDP	0.3V to LDO+0.3V
BST referred to LX	0.3V to +7V
SCL, SDA to GNDP	0.5V to +7V
Maximum Operating Junction temperature	+125°C
Storage temperature range	

**NOTE**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **RECOMMENDED OPERATING RANGE**

VBUS, VDC to GNDP	3.9V to 14V
SDA, SCL, PS, STAT, PG#, CE#, PB#, THM, IRQ, ILMT	0V to LDO
VSYS, VBAT	
Operating temperature range (ambient)	

## **ELECTRICAL CHARACTERISTICS**

 $V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} > V_{SLEEP}$ ,  $T_J = -40^{\circ}C$  to +125°C and  $T_J = 25^{\circ}C$  for typical values (unless otherwise noted)

	PARAMETER	TEST	MIN	TYP	MAX	UNITS
QUIESCENT	CURRENTS	•				
		VVBUS = 5 V, High-Z mode, no battery, battery monitor disabled		15	30	μA
I <sub>VBUS</sub>		VVBUS = 12V, High-Z mode, no battery, battery monitor disabled		30	50	μA
	Input supply current (VBUS)	VVBUS > VUVLO, VVBUS > VBAT, converter not switching		1.5	3	mA
		VVBUS > VUVLO, VVBUS > VBAT, converter switching, VBAT=3.2V, Isys=0A		3		mA
		VVBUS > VUVLO, VVBUS > VBAT, converter switching, VBAT=3.8V, ISYS=0A		3		mA
VBUS/BAT P	OWER UP	·				
V <sub>VBUS_OP</sub>	VBUS operating range		3.9		14	V
V <sub>VBUS_UVLOZ</sub>	VBUS for active I <sup>2</sup> C, no battery	V <sub>VBUS</sub> rising	3.6			V
V <sub>SLEEP_F</sub>	Sleep mode falling threshold	$V_{VBUS}$ falling, $V_{VBUS-VBAT}$	25	65	120	mV
V <sub>SLEEP_R</sub>	Sleep mode rising threshold	V <sub>VBUS</sub> rising, V <sub>VBUS-VBAT</sub>	130	250	370	mV
	VBUS over-voltage rising threshold	V <sub>VBUS</sub> rising	14		15	V
V <sub>ACOV</sub>	VBUS over-voltage falling threshold	V <sub>VBUS</sub> falling	13.5		14.5	
VBAT_UVLOZ	Battery for active I <sup>2</sup> C, no VBUS	V <sub>BAT</sub> rising	2.3			V



## **ELECTRICAL CHARACTERISTICS (Continued)**

 $V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} > V_{SLEEP}$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  and  $T_J = 25^{\circ}C$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>ON(HSFET)</sub>	Internal top switching MOSFET on	$T_J = -40^{\circ}C - 85^{\circ}C$		22		mΩ
(INCINCIPACITY)	resistance between VDC and LX	TJ = -40°C – 125°C		22		
P	Internal bottom switching MOSFET on-resistance between	$T_J = -40^{\circ}C - 85^{\circ}C$		24		mΩ
R <sub>ON(LSFET)</sub>	LX and PGND	$T_{J} = -40^{\circ}C - 125^{\circ}C$		24		11122
V <sub>FWD</sub>	BATFET forward voltage in supplement mode	Battery discharge current 10mA		30		mV
BATTERY CHA	RGER					
V <sub>BAT_RANGE</sub>	Typical charge voltage range	V <sub>BAT</sub>	3.84		4.608	V
VBATRG_STEP	Typical charge voltage step			16		mV
$V_{\text{BAT}\_\text{REG}\_\text{ACC}}$	Charge voltage regulation accuracy	V <sub>BAT</sub> = 4.208V or 4.352V	-0.5		0.5	%
I <sub>CHG_REG_RANGE</sub>	Typical fast charge current regulation range	I <sub>CHG</sub>	0		3000	mA
I <sub>CHG_REG_STEP</sub>	Typical fast charge current regulation step			64		mA
	Fast charge current regulation accuracy	$V_{BAT} = 3.8V, I_{CHG} = 128mA$ $T_{J} = -40^{\circ}C - 85^{\circ}C$	-20		20	
$I_{\rm ICHG\_REG\_ACC}$		$V_{BAT} = 3.8V, I_{CHG} = 256mA$ $T_{J} = -40^{\circ}C - 85^{\circ}C$	-10		10	%
		$V_{BAT} = 3.8V, I_{CHG} = 1792mA$ $T_{J} = -40^{\circ}C - 85^{\circ}C$	-5		5	
VBATLOWV	Battery LOWV falling threshold	Fast charge to precharge, REG06[1] = 1	2.6	2.8	2.9	V
-	Battery LOWV rising threshold	Precharge to fast charge, REG06[1] = 0	2.8	3.0	3.1	V
IPRECHG RANGE	Precharge current range	I <sub>PRECHG</sub>	64		1024	mA
PRECHG_STEP	Typical precharge current step		64	64	1024	mA mA
I <sub>TERM RANGE</sub>	Termination current range Termination current step	I <sub>TERM RANGE</sub> Iterm step	64	64	1024	mA
V <sub>BATSHORT</sub>	Battery Short Voltage	V <sub>BAT</sub> falling	-	2		V
VBATSHORT_HYST	Battery Short Voltage hysteresis	V <sub>BAT</sub> rising		200		mV
I <sub>SHORT</sub>	Battery short current (trickle current)	V <sub>BAT</sub> <2.2V		100		mA
V <sub>RECHG</sub>	Recharge threshold below VBATREG	V <sub>BAT</sub> falling, REG06[0] = 0 V <sub>BAT</sub> falling, REG06[0]=1		100 200		mV mV
R <sub>ON(BATFET)</sub>	SYS-BAT MOSFET on-resistance	$T_J = 25^{\circ}C$		12		mΩ
IBATLOAD	Battery discharge load current	V <sub>BAT</sub> =4.2V		15		mA
ISYSLOAD	System discharge load current	V <sub>SYS</sub> =4.2V		30		mA
Input Voltage/C	Current Regulation					
VINDPM_RANGE	Typical input voltage range	V <sub>BUS</sub>	3.9		15.3	V
VINDPM_STEP	Typical input voltage regulation step	V <sub>VBUS_STEP</sub>		100		mV
VINDPM_ACC	Input voltage regulation accuracy	VINDPM=4.4V	-3		3	%
IINDPM_RANGE	Typical input current range	ILMTSET	100		2400	mA
IINDPM_STEP	Input current regulation step	ILMTSET_STEP	50			mA
	Input current regulation accuracy,	USB500,ILIMSET(REG00[5:0])=500mA Adapter 1.5A,	440		500	mA
_	V <sub>BAT</sub> =5V, current pulled from LX	ILIMSET(REG00[5:0])=1500mA	1300		1500	mA
K <sub>ILIM</sub>	I <sub>INMAX</sub> =K <sub>ILIM</sub> /R <sub>ILIM</sub>	Input current regulation by ILIM pin=1.5A	320		390	AxΩ



## **ELECTRICAL CHARACTERISTICS (Continued)**

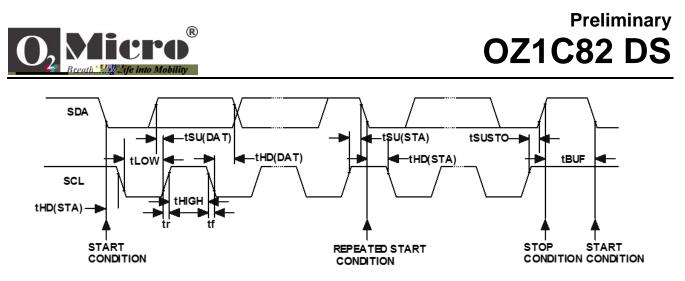
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	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic I/O	pin Characteristics (CE#,PS,PB#)	•				
VIH	Input high threshold level		1.3			V
VIL	Input low threshold level				0.4	V
I <sub>IN_BIAS</sub>	High level leakage current	Pull-up rail 1.8V			1	uA
		Battery only mode		VBAT		
V <sub>PB#</sub>	Inter PB# pull-up	V <sub>VBUS</sub> =9V		5.1		V
		V <sub>VBUS</sub> =5V		4.8		
R <sub>PB#</sub>	Internal PB# pull-up resistance			1		MΩ
Logic I/O	pin Characteristics (IRQ,STAT,PG#)	•				
V <sub>OL</sub>	Output low threshold level	Sink current=5mA			0.4	V
OUT_BIAS	High level leakage current	Pull-up rail 1.8V			1	uA
I <sup>2</sup> C Interfa	ce (SCL,SDA)	· · ·				
V <sub>IH</sub>	Input high threshold level, SCL and SDA	Pull-up rail 1.8V	1.3			V
VIL	Input low threshold level, SCL and SDA	Pull-up rail 1.8V			0.4	V
Vol	Output low voltage level	Sink current=5mA			0.4	V
IBIAS	High level leakage current	Pull-up rail 1.8V			1	uA

### **Timing Requirements**

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
I <sup>2</sup> C Interface	e (SCL,SDA)			
fscL	SCL clock frequency		400 <sup>Note 1</sup>	kHz
Battery Ove	r-voltage Protection	·	· · · · ·	
t <sub>BATOVP</sub>	Battery over-voltage deglitch time to disable charge		1	us
Battery Cha	rger	·	·	
<b>t</b> RECHG	Recharge deglitch time		20 <sup>Note 1</sup>	ms
Battery mor	nitor			
t <sub>CONV</sub>	Conversion time	CONV_RATE(REG02[6])=1	1000 <sup>Note 1</sup>	ms
PB# and Sh	ipping Timing			
t <sub>SHIPMODE</sub>	PB# low time to turn on BATFET and exit ship mode	T <sub>J</sub> =-10°C-60°C	1.75 <sup>Note 1</sup>	sec
t <sub>QON_RST</sub>	PB# low time to enable full system reset	T <sub>J</sub> =-10°C-60°C	15 <sup>Note 1</sup>	sec
t <sub>BATFET_RST</sub>	BATFET off time during full system reset	T <sub>J</sub> =-10°C-60°C	450 <sup>Note 1</sup>	ms
t <sub>SM_DLY</sub>	Enter ship mode delay	T <sub>J</sub> =-10°C-60°C	12.5 <sup>Note 1</sup>	sec
Digital Cloc	k and Watchdog Timer			
f <sub>LPDIG</sub>	Digital low power clock	LDO disabled	30	kHz
f <sub>DIG</sub>	Digital clock	LDO enabled	1000	kHz
t <sub>WDT</sub>	Watchdog time	Watchdog (REG07[5:4]=01),LDO enabled	40 <sup>Note 1</sup>	sec

Note 1: all the items with Note 1







### **FUNCTIONAL DESCRIPTION**

#### **Device power-on-reset (POR)**

The internal bias circuit is powered from the higher voltage between VBUS and VBAT. When VBUS rises above  $V_{VBUS\_UVLOZ}$  or VBAT rises above  $V_{VBAT\_UVLOZ}$ , the sleep comparator, battery depletion comparator and BATFET driver are active. I<sup>2</sup>C interface is ready for communication and all registers are reset to default value. The host can access all the registers after POR.

# Device powered up from battery without input source

When only battery is present and the battery voltage is above the depletion threshold ( $V_{BAT_DPLZ}$ ), the BATFET turns on and connects battery to system. The LDO stays off to minimize the quiescent current. The low  $R_{DS(ON)}$  of BATFET and low quiescent current on VBAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharging current through BATFET.

When the system is overloaded or shorted(I<sub>BAT</sub>>I<sub>BATFET\_OCP</sub>), the device turns off BATFET immediately and sets BATFET\_DIS bit to indicate BATFET is disabled until input source is plugged in again or BATFET is re-enabled again.

#### Device powered up from input source

When an input source is plugged in, the device checks the input source voltage to turn on LDO and all the bias circuit. It detects and sets the input current limit before the buck converter is started when AUTO\_DPDM\_EN bit is set. The power up sequence from input source is as listed:

- 1. Power up LDO
- 2. Input source type detection based on PS to set the default input current limit register and input source type.
- 3. Input voltage limit threshold setting
- 4. Converter power up

#### Power up LDO regulation

LDO supplies the internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to THM external resistors. The pull-up rail of STAT and PG# can be connected to LDO as well. The LDO is enabled when all the below conditions are valid:

- 1. VBUS above the  $V_{VBUS_UVLOZ}$
- 2. VBUS above  $V_{BAT}+V_{SLEEPZ}$  in buck mode
- 3. After 220ms delay is completed

If one of the above conditions is not valid, the device is in high impedance mode (**HIZ**) with LDO off. The device draws less than  $I_{VBUS\_HIZ}$  from VBUS during **HIZ** state. The battery powers up the system when device is in **HIZ**.

#### **Poor Power Qualification**

After LDO powers up, the input source has to meet the following requirements in order to start the buck converter.

- 1. VBUS voltage below V<sub>ACOV</sub>
- 2. VBUS voltage above  $V_{VBUSMIN}$

Once the input source passes all the conditions above, the status register bit VBUS\_GD is set high and IRQ pin sends a pulse to the host, if the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

# Input current limit detection and input current limit setting

OZ1C82 runs VBUS input current limit detection by PS pin after VBUS is plugged in and LDO powers up, and then sets VBUS input current limit default value into IINLIM register that can be read by host as below:

Table 1: IINLIMIT detection

Input detection	PS	IINLIM	0x0Bh
		(mA)	bit[7:5]
USB SDP	High	500	001
(USB500)	-		
Adapter	Low	3250	010

Anytime, host can set IINLIM register 0x00h by  $I^2C$ . The charger input current is always limited by the lower of IINLIM or ILIM pin.

# Input voltage limit detection and input voltage limit setting (VINDPM Threshold)

OZ1C82 supports wide range of input voltage limit (3.9V-14V) for high voltage charging and provides two methods to set input voltage limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM

By setting FORCE\_VINDPM bit to 1, the VINDPM threshold setting algorithm is disabled. Register VINDPM is writeable and allows host to set the absolute threshold of VINDPM function.

2. Relative VINDPM

When FORCE\_VINDPM bit is 0(default), the VINDPM threshold setting algorithm is enabled. The VINDPM register is read only and the charger controls the register by using VINDPM threshold setting algorithm. The algorithm allows a wide range of adapter (VvBUS\_OP) to be used with flexible VINDPM threshold.

#### Converter power up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If the battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rails ramp up. When the system rail is below 2.2V, the input current limit is



forced to the lower of 100mA or ILIM pin. After the system rises above 2.2V, the device limits the input current to the lower value of ILIM pin and IINLIM register. In order to improve the light–load efficiency, the device enters skip mode at light load.

#### Input current optimizer (ICO)

OZ1C82 provides input current optimizer (ICO) to indentify maximum power point without overload the input source. The algorithm automatically identifies maximum input current limit of power source without entering VINDPM to avoid input source overload.

The feature is disabled by default (ICO\_EN=0) and can be enabled by setting ICO\_EN bit to 1. After the input source is addited by end BCO in the addited and the input source by setting The algorithm can also be forced to execute by setting FORCE\_ICO bit regardless of input source type 794(w)1.064 Tm[()] TJETBT1 0 051 250.37 499.2i Tm[(I-5(i)-4(n)] TJETBT1 0 051 250.37



For safe operation, the host should set the maximum allowed regulation voltage register and the minimum resistance compensation.

# JEITA guideline compliance in charge mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charging current and high charging voltage at certain low and high temperature ranges.

The OZ1C82 continuously monitors battery temperature by measuring the voltage between the THM pin and ground, typically determined by a negative temperature coefficient thermistor (NTC) and an external voltage divider. The OZ1C82 compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle; the voltage on THM pin must be within the VT1 to VT5 thresholds. If THM voltage exceeds the T1–T5 range, the controller suspends charging and the LED connecting to ST pin



1. VBUS source identified (through PS detection and OTG pin)

- 2. VBUS power source good
- 3. VBUS above battery (not in sleep)
- 4. VBUS removed or below  $V_{ACOV}$  threshold
- 5. VBUS above V<sub>VBUSMIN</sub> (typical 3.8V) (not a poor source)
- 6. Charge Complete
- 7. Any fault event in REG0C

When a fault occurs, OZ1C82 sends out IRQ and keeps the fault state in REG0C until the host reads REG0C. Before the host reads REG0C and all the faults are cleared, OZ1C82 wouldn't send any IRQ upon new faults. To read the current fault status, the host has to read REG0C twice consecutively. The 1<sup>st</sup> read reports the pre-existing fault status and the 2<sup>nd</sup> read reports the current fault status.

#### **Safety Timer**

If the safety timer is expired, the switch between VSYS and VBAT is off to prevent further charging, and LED blinks on and off with 1Hz frequency. The buck converter keeps enabled to supply system. CHRG\_FAULT bits set to 11 and IRQ will generate 250µs low pulse. In charging mode, fast charging safety timer is programmed by REG07 [2:1], wake up timer is default 4hours. The safety timer can be disabled by setting EN\_TIMER=0

During input voltage, current or thermal regulation, the safety timer counts at half clock rate because the real charge current could be lower than the register setting. This half clock rate feature can be disabled by setting EN\_TMR2X=0

#### **VBUS OVP (ACOV)**

When VBUS voltage exceeds  $V_{ACOV}$ , OZ1C82 will stop switching immediately. During ACOV, the fault register CHRG\_FAULT bits set to 01 and an IRQ asserts to the host.

#### System OVP

When over voltage happens for system, both buck converter and BATFET between VSYS and VBAT are off. The charging will be automatically restarted when OVP condition disappears.

#### System OCP

When the system is shorted or significantly overloaded ( $I_{BAT}$ > $I_{BATOP}$ ) so that its current exceeds the over-current limit, OZ1C82 latches off BATFET. BATFET Enable Section (Exit shipping mode) can reset the latch-off condition and turn on BATFET.

#### **Thermal Protection in Buck Mode**

OZ1C82 monitors the internal junction temperature  $T_J$  to avoid overheat and limits IC surface temperature in buck mode. When  $T_J$  exceeds the preset thermal regulation limit by TREG bits (REG08[1:0]), the charge current would be lowered down. During thermal regulation, the actual charging current is usually below the setting charging current. So termination is disabled, the safety timer runs at half the clock rate, and the status register THERM\_STAT bit goes high.

OZ1C82 has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds  $T_{SHUT}$ . The fault register CHRG\_FAULT is set to 10 and IRQ is asserted to the host. The converter and BATFET will be enabled to recover when IC temperature lower than  $T_{SHUT_HYST}$ .

#### **Battery Overvoltage Protection (BATOVP)**

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charging function is disabled immediately. And the fault register BAT\_FAULT bit goes high.

#### **Battery Over-Discharge Protection**

When battery is discharged below  $V_{BAT_DPL}$ , BATFET will be turned off to protect battery from over discharge. Battery will recover to be normal when an input source detected at VBUS. When an input source is plugged in, BATFET turns on, and the battery is charged with I<sub>SHORT</sub> (typical 100mA) current when  $V_{BAT}$ </br>Ver battery or pre-charge current as set in IPRECHG register when the battery voltage is between VBATSHORT and VBATLOWV.

#### **Battery Monitor**

OZ1C82 can report  $V_{VBUS}$ ,  $V_{BAT}$ ,  $V_{SYS}$ , thermistor ratio, and charging current in battery monitor registers (REG0E-REG12). The battery monitor can be configured as two conversion modes by CONV\_RATE bit (REG02[6]): one-shot conversion (default) and 1 second continuous conversion.

For one-shot conversion (CONV\_RATE=0), the CONV\_START bit needs to be set 1 to start the conversion. And CONV\_START bit is cleared by OZ1C82 when conversion is completed. The conversion result is ready after  $t_{CONV}$  (maximum 1 second)

For continuous conversion (CONV\_MODE=1), the CONV\_START needs to be set 1 to start the conversion. During active conversion, the CONV\_START keeps 1 to indicate conversion is in progress. The battery monitor provides conversion result every 1 second automatically. The battery monitor exits continuous conversion mode when CONV\_START is cleared.

#### **BATFET Disable Mode (Shipping Mode)**

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, OZ1C82 can turn off BATFET by setting BATFET\_DIS=1



so that the system voltage is zero to minimize the battery leakage current. And BATFET can turn off immediately or delay by  $t_{SM_DLY}$  as defined by BATFET\_DLY bit.

#### **BATFET Enable (Exit Shipping Mode)**

BATFET can be enabled to restore system power by one of the following events:

- 1. Plug in adapter
- 2. Clear BATFET\_DIS bit

3. Set REG\_RST=1 to reset all the registers including BATFET DIS bit to default 0

4. A logic high to low transition on PB# with t<sub>SHIPMODE</sub> deglitch time to enable BATFET to exit shipping mode

#### Standby Mode Charge

In standby mode, there is no  $I^2C$  command to be sent by host when both VBUS and battery are active, PS and CE# are low active; in this case, OZ1C82 can also complete a charging cycle automatically with default charging parameters are listed in the following table.

Table 3: Default charger parameters

Standby mode	Default charging parameters
Charging Voltage	4.208V
Charging Current	2048A
Wake up Current	128mA
Termination current	256mA
Recharging threshold	100mV
Wake up timer	4 hours
CC Charge timer	12 hours
Wake up threshold	3V
V <sub>SYSMIN</sub> threshold	3.5V

Anytime, host can access OZ1C82 and change the charger parameters by  $I^2C$  according to customer's charging requirements



#### **Constant Voltage and Constant Current Operation**

As shown in Figure 5, the charger in OZ1C82 uses six error amplifiers: EA1 for the adapter current limitation, EA2 for charging voltage regulation, EA3 for charging current regulation, and EA4 for VBUS voltage regulation, EA5 for system voltage regulation, and EA6 for thermal regulation. The outputs of these four error amplifiers are tied to the COMP pin for compensation.

The output of the adapter current-sense amplifier is connected to the error amplifier EA1. EA1's output is connected to the COMP pin. Therefore, whenever the AC adapter current limit is exceeded, EA1 output will control the COMP voltage. The charger's duty cycle will be reduced until the total adapter current falls within its limit value. In a constant current regulation operation, the error amplifier EA3 will control the COMP pin voltage. The circuit operates to regulate the charger output current according to the desired current setting by  $I^2C$  programming with ±5% accuracy.

In a constant voltage operation, the error amplifier, EA2 will control the COMP pin. The circuit operates to regulate the charger output voltage according to the desired voltage setting by  $I^2C$  programming with ±0.5% accuracy.

In a VBUS voltage regulation operation, the error amplifier, EA4 will control the COMP pin. The circuit operates to regulate the VBUS input voltage according to the VBUS VLMT voltage setting by  $I^2C$  programming with ±3% accuracy.

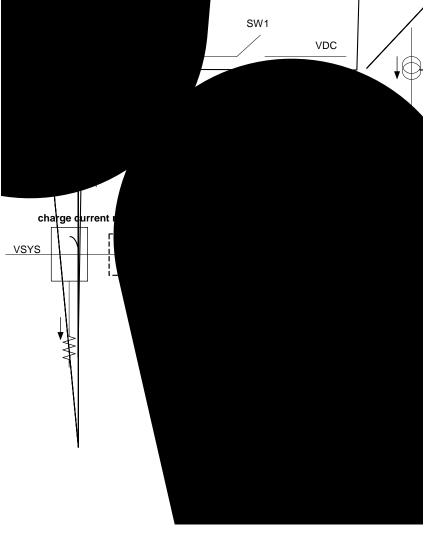


Figure 5: Voltage, Current and Thermal regulation loops



Preliminary OZ1C82 DS

#### **Serial Interface**

The device uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG14. Register read beyond REG14 (0x14) returns 0xFF. The I2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

#### a) Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

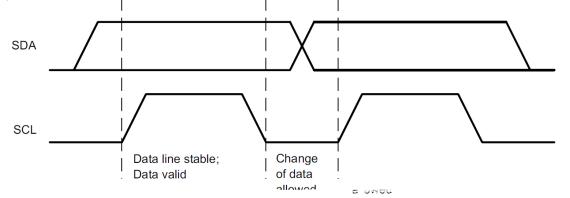
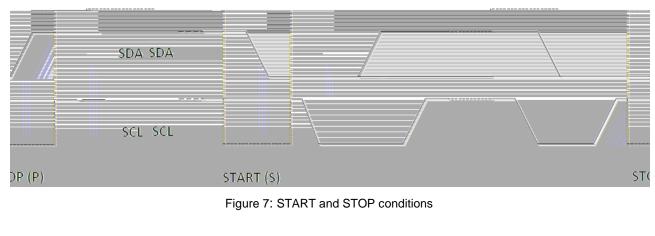


Figure 6: Bit Transfer on the I<sup>2</sup>C Bus

#### b) START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

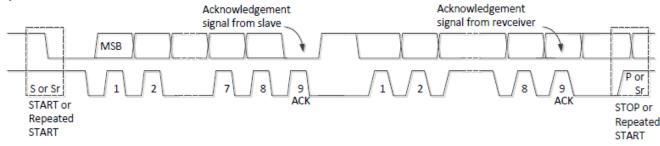






#### c) Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.





#### d) Acknowledge (ACK) and Not Acknowledge (NACK)

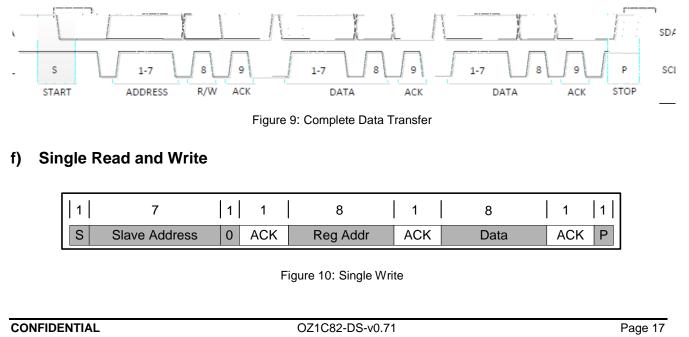
The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9<sup>th</sup> clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9<sup>th</sup> clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

#### e) Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).





1	7	1  1	8	1  1	7	1  1
S	Slave Address	0 ACK	Reg Addr	ACK S	Slave Address	1 ACK
					8	1  1
					Data	NACK P

Figure 11: Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

#### g) Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG14 except REG0C.

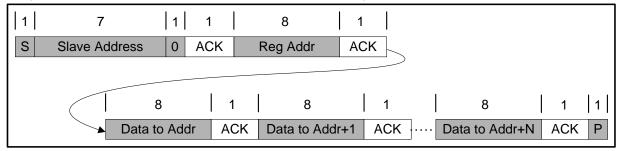


Figure 12: Multi-Write

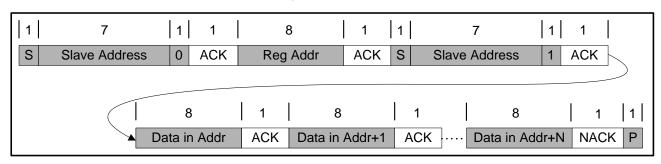


Figure 13: Multi-Read

REGOC is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REGOC reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REGOC for the second time. The only exception is NTC\_FAULT which always reports the actual condition on the TS pin. In addition, REGOC does not support multi-read and multi-write.



### Host mode and default mode

The OZ1C82 is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charge is in default mode, WATCHDOG\_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG\_FAULT bit is LOW.

After POR, the device starts in default mode with watchdog timer expired, or default mode, all the registers are in the default settings.

In default mode, the device keeps charging the battery with 12-hour fast charging safety timer. At the end of 12 hour, the charging is stopped and the buck converter continues to operate to supply system load. Any write command to the device will switch the default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WATCHDOG\_RST bit before watchdog timer expires(WATCHDOG\_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits=00.

When the watchdog timer (WATCHDOG\_FAULT bit=1) is expired, the device returns to default mode and all registers are reset to default value except IINLIM, VINDPM\_OS, BATFET\_RST\_EN, BATFET\_DLY and BATFET\_DIS bits.

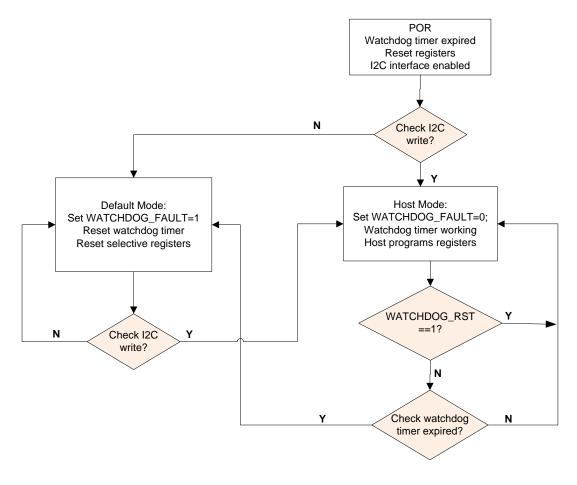


Figure 14: Watchdog timer for host mode and default mode





## **REGISTER MAP**

Register index				Bit Nu	umber					
(hex)										
	EN_HIZ	EN_ILIM			IINI	_IM[5:0]				
	Reserved	Reserved	Reserved			VINDPM_OS[4:0]				
	CONV_START	CONV_RATE	Reserved	ICO_EN	Reserved	Reserved	FORCE_DPDM	AUTO_DPDM_EN		
	BAT_LOADEN	WD_RST	Reserved	CHG_CONFIG		SYSMIN[2:0]		Reserved		
	EN_PUMPX				ICHG[6:0]					
		IPREC	HG[3:0]			ITERM[3:0]				
			VREC	G[5:0]			BATLOWV	VRECHG		
	EN_TERM Reserved WATCHD		DOG[1:0]	EN_TIMER	CHG_TIMER[1:0]		JEITA_ISET (0°C-10°C)			
		BAT_COMP[2:0]			VCLAMP[2:0]			EG[1:0]		
	FORCE_ICO	TMR2X_EN	BATFET_DIS	JEITA_VSET (45°C-60°C)	BATFET_DLY	BATFET_RST_EN	PUMPX_UP	PUMPX_DN		
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		
		VBUS_STAT[2:0]		CHRG	_STAT	PG_STAT	Reserved	VSYS_STAT		
	WATCHDOG_ FAULT	Reserved	CHRG_	FAULT	BAT_FAULT	NTC_FAULT[2:0]				
	FORCE_VINDPM				VINDPM[6:0]					
	THERM_STAT				BATV[6:0]					
	Reserved	SYSV[6:0]								
	Reserved				TSPCT[6:0]					
I		•			VBUSV[6:0]					

VBUS\_GD

VBUSV[6:0]



### **DETAILED REGISTER INFORMATION**

This part describes the register definition and configuration for OZ1C82.

The following describes the register definition and configuration for charger module. Its I<sup>2</sup>C slave write address is D6H and the slave read address is D7H.

	7	EN HIZ	R/W	By REG_RST	0	Enable HIZ	Zmode
	'			By Watchdog	0	0 Disable	e(default) 1 Enable
	6	EN_ILIM	R/W	By REG_RST	1	Enable ILIN	
	-			By Watchdog	1	0 Disable	
	5	IINLIM[5]	R/W	By REG_RST	0	1600mA	Input Current Limit
	4	IINLIM[4]	R/W	By REG_RST	0	800mA	Offset:100mA
00	3	IINLIM[3]	R/W	By REG_RST	1	400mA	Range:100mA(000000)—3.25A(111111)
	2	IINLIM[2]	R/W	By REG_RST	0	200mA	Default:001000(500mA)
	1	IIN⊔M[1]	R/W	By REG_RST	0	100mA	(Actual input current limit is the lower of I2Cor ILIM pin)
							IINLIM bits are changed automatically after input source type
	0		R∕W	By REG_RST	0	50mA	detection is completed
	Ŭ						PSE = Hi (USB500) = 500 mA
							PSEL=L0=3.25A
	_	<u> </u>					
	7	Reserved	R	N/A		Always re	
	6	Reserved	R	N/A		Always rea	
	5	Reserved	R	N/A		Always rea	
	4	VINDPM_OS[4]	R/W	By REG_RST	0	1600mV	Input Voltage Limit Offset
	3	VINDPM_OS[3]	R/W	By REG_RST	0	800mV	Default: 600mV (00110)
	2	VINDPM_OS[2]	R/W	By REG_RST	1	400mV	Range: 0mV—3100mV
	1	VINDPM_OS[1]	R/W	By REG_RST	1	200mV	Minimum VINDPM threshold is clamped at 3.9V
							Maximum VINDPM threshold is clamped at 15.3V
							When VBUSat no Load is ≤6V, the VINDPM_OS is used to
	0	VINDPM_OS[0]	R/W	By REG_RST	0	100mV	calculate VINDPM threshold
							When VBUSat no Load is > 6V, the VINDPM_OSmultiple by 2 is
							used to calculate VINDPM threshold.
						ADCConve	ersion Start Control

ADC Conversion Start Control

0-ADC conversion not active (default)

7 CONV\_START R∕W

By REG\_RST By Watchdog

0

1-Start ADC Conversion This bit is read-only when CONV\_RATE = 1. T04.06 q286.97 109.46 337.Tf1 0 (



	7	BATLOAD EN	R∕W	By REG_RST	0	Battery	.oad (IBATLOAD) Enable
	'		14.00	By Watchdog	0		bled (default) 1 Enabled
	6	WD_RST	R∕W	By REG_RST	0		hdog Timer Reset
		_		By Watchdog	0		nal (default) 1 Reset (Back to 0 after timer reset)
	5	Reserved	R	N/A		Alwaysr	
	4	CHG CONFIG	R∕W	By REG_RST	1	Charge E	nable Configuration
03	4		14.00	By Watchdog	-	0 Char	ge Disable 1 Charge Enable(default)
00	3	SYS_MIN[2]	R/W	By REG_RST	1	0.4V	
	Ŭ	010_1111 ([2]		By Watchdog		0.11	Minimum System Voltage Limit
	2	SYS_MIN[1]	R/W	By REG_RST	0	0.2V	Offset: 3.0V
			-	By Watchdog	-	-	Range 3.0V-3.7V
	1	SYS_MIN[0]	R/W	By REG_RST	1	0.1V	Default: 3.5V
	_		_	By Watchdog			
	0	Reserved	R	N/A		Alwaysr	eads 0
							Dulas Osstas   Espirit
	_		DUM	By REG_RST	<u> </u>		Pulse Control Enable
	7	EN_PUMPX	R∕W	By Watchdog	0		ble Current pulse control (default)
	<u> </u>			, ,		u—≞nab	le Current pulse control (PUMPX_UP and PUMPX_DN)
	6	ICHG[6]	R/W	By REG_RST	0	4096mA	
				By Watchdog			_
	5	ICHG[5]	R/W	By REG_RST	1	2048mA	Fact Channel Connect Line's
				By Watchdog By REG_RST			Fast Charge Current Limit
	4	ICHG[4]	R/W		0	1024mA	Offset:0mA
				By Watchdog			Range:0mA(0000000)—5056mA(1001111)
	3	ICHG[3]	R/W	By REG_RST By Watchdog	0	512mA	Default:2048mA(0100000) Note:
				By REG_RST			ICHG=0000000(0mA) disable charge
	2	ICHG[2]	R/W	By Watchdog	0	256mA	ICHG>1001111(5056mA) is damped to register value
				By REG_RST			1001111(5056mA)
	1	ICHG[1]	R/W	By Watchdog	0	128mA	
				By REG_RST			-
	0	ICHG[0]	R/W	By Watchdog	0	64mA	
				i, i i i i i i i i i i i i i i i i i i			
	-		D()	By REG RST	~	= 1	
	7	IPRECHG[3]	R/W	By Watchdog	0	512mA	
	6		D() 4 (	By REG_RST	6	050 /	Pre-charge Ourrent Limit
	6	IPRECHG[2]	R/W	By Watchdog	0	256mA	Offset:64mA
	_		DUM	By REG_RST	0	400	Range:64mA—1024mA
	5	IPRECHG[1]	R/W	By Watchdog	0	128mA	Default:128mA (0001)
	4			By REG_RST		C 4ree A	
	4	IPRECHG[0]	R/W	By Watchdog	1	64mA	
	3		R∕W	By REG_RST	0	512mA	
	3	ITERM[3]		By Watchdog	U	SIZIIIA	
	2	ITERM[2]	R/W	By REG_RST	0	256mA	Termination Ourrent Limit
				By Watchdog	U	200MA	Offset:64mA
	1	ITERM[1]	R/W	By REG_RST	1	128mA	Range:64mA—1024mA
			14.00	By Watchdog	-	120MA	Default:256mA (0011)
	0	ITERM[0]	R∕W	By REG_RST	1	64mA	
	Ŭ		14.00	By Watchdog		5-1103	



7         VREQ5[]         RW         By PREQ RST By PREQ RST Charge Voltage Limit Of test: 34/4 VCLS-110000 (4.608V) is damped to register value 11000 (4.608V)           1         BATLOWV By PREQ RST By PREQ RST D D VREDHG         1         64mV D D VREDHG By PREQ RST D D VREDHG         D Carge Voltage Limit O D VREDHG         0           0         VRECHG PV BY PREQ RST D D VREDHG         RVW By PREQ RST D D VREDHG         1         16mV D D VREDHG         D Carging Terehold Offset (Biolow Charge Voltage Limit) D - 100mV (Verac) Delow VREG (REGOR[7.2]) D - 00mV (Verac) DElow VRE							
b         VREA(3)         RW         By Watchdog         1         Zonu         Utility Strategithm           6         VREQ(3)         RW         By RSLST         Diversition         Diversition         Diversition           4         VREQ(2)         RW         By RSLST         1         64mV         Pressition           3         VREQ(1)         RW         By RSLST         1         64mV         Note:           2         VREQ(0)         RW         By RSLST         1         64mV         Note:           1         BATLDMV         RW         By RSLST         1         16mV         Note:           1         BATLDMV         RW         By RSLST         Detery Pre-charge to Fast Charge Threshold         0           1         BATLDMV         RW         By RSLSTS         0         Detarty Pre-charge to Fast Charge Threshold         0           0         VRECHS         RW         By RSLSTS         0         Detarty Pre-charge to Fast Charge Threshold         0           0         VRECHS         RW         By RSLSTS         0         On-craiging Termination Erable         0           0         VRECHS         RW         By RSLSTS         0         On-craiging Termination Erable<	7	VREG[5]	R∕W	By Watchdog	0	512mV	
5         VFEG[3]         PVW         By PEG_PST         0         128mV         Parge_34V-4.000V(1000)           4         VFEG[2]         PVW         By REG_PST         1         64mV         Pres_34V-4.000V(10111)           3         VFEG[1]         PVW         By REG_PST         1         64mV         Vete(0)         4.608V)           2         VFEG[0]         PVW         By REG_PST         1         32mV         (4.608V)           1         BATLOWV         PVW         By REG_PST         1         10mV         (4.608V)           1         BATLOWV         PW By Vetchdog         1         16mV         (4.608V)         (4.608V)           0         VFECHG         PV RG_PST         1         Battery Pe-charge Threshold Offset         (6.000 Charge PV/Respect)         (4.608V)           0         VFECHG         PV RG_PST         0         Datable Vetarge Threshold Offset         (6.000 Charge PV/Respect)         (7.000)         (4.0000)         (6.000 Charge PV/Respect)         (7.000)         (6.000 Charge PV/Respect)         (7.000)         (6.000 Charge PV/Respect)         (7.000)         (7.000)         (7.000) <td< td=""><td>6</td><td>VREG[4]</td><td>R/W</td><td>By REG_RST</td><td>1</td><td>256mV</td><td></td></td<>	6	VREG[4]	R/W	By REG_RST	1	256mV	
4         VREG(2)         RVW         By Watchdog By Watchdog         1         64mV GW By Watchdog         Note: VOHG-10000 (4.608V) is damped to register value 11000 (4.608V)           2         VREQ(1)         RVW         By REG, RST By Watchdog         1         1         1         1         0         VHG-10000 (4.608V) is damped to register value 11000 (4.608V)           1         BATLOWV         RVW         By REG, RST By Watchdog         1         1         1         1         1         1         1         0         -2.8V         -13.0V (default)         -2.8V         -3.0V (default)	5	VREG[3]	R/W	/ _	0	128mV	Range:3.84V—4.608V(110000)
3         VREQ1         RVW         By REG, RST         1         32mV         (4.608V)           2         VREQ0         RVW         By REG, RST         1         16mV         1         6.00V           1         BATLOWV         RVW         By REG, RST         1         16mV         0         0         0         WREDHER         NV         By REG, RST         1         1         0         0         0         0         0         By REG, RST         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0         0	4	VREG[2]	R/W	By Watchdog	1	64mV	Note:
2         VREQU         PVW         By Watchdog         1         Intro           1         BATLOWV         RVW         By REG_RST By Watchdog         1         Battery Pre-charge to Fast Charge Threshold           0         VRECHG         RVW         By REG_RST By Watchdog         1         Battery Pre-charge to Fast Charge Threshold Offset (Below Charge Voltage Limit)           0         VRECHG         RVW         By REG_RST By Watchdog         0         Onarging Termination Enable 0         0           7         BN_TERM         RW         By REG_RST By Watchdog         1         Onarging Termination Enable 0         0           6         Beserved         R         N/A         Alwaysreads0         1         -Dasable         1         -Dasable finer Satting           4         WATCHDOG(1)         RVW         By REG_RST By Watchdog         1         0         -Dasable finer Satting           2         CHG_TIMER(1)         RVW         By REG_RST By Watchdog         1         0         -Dasable finer Satting           2         CHG_TIMER(1)         RVW         By REG_RST By Watchdog         1         0         -Dasable finer Satting           2         CHG_TIMER(1)         RVW         By REG_RST By Watchdog         1         -Dasable finer Satting </td <td>3</td> <td>VREG[1]</td> <td>R∕W</td> <td>By Watchdog</td> <td>1</td> <td>32mV</td> <td></td>	3	VREG[1]	R∕W	By Watchdog	1	32mV	
1         BATLOWV         RVW         By Red, RSI By Watchdog         1         0         -2.8V           0         VREOHG         RVW         By REG, RST By Watchdog         0         Battery Recharge Threshold Offset (Below Charge Voltage Limit)           7         EN_TERM         RVW         By REG, RST By Watchdog         0         Oraging Termination Enable 0         0           6         Reserved         R         N/A         Alwaysreads0         1         0           4         WATCHDOG(1)         RVW         By REG, RST By Watchdog         1         0         Dasble         1         Enable (default)           3         EN_TIMER         RVW         By REG, RST By Watchdog         1         0         Dasble varchable (default)           2         CHG_TIMER(1)         RVW         By REG, RST By Watchdog         1         0         Dasble varchable (default)           2         CHG_TIMER(1)         RVW         By REG, RST By Watchdog         1         0         Dasble varchable (default)           2         CHG_TIMER(1)         RVW         By REG, RST By Watchdog         1         0         Dasble (default)           3         BL_TIMER(1)         RVW         By REG, RST By Watchdog         1         0         Dasble	2	VREG[0]	R/W		1		
0         VRECHG         RW         by REG_RST By Watchdog         0         (Below Charge Voltage Limit) 0100mV (V <sub>sect</sub> ) below VREG (REGOR[7:2]) (default) 1200mV (V <sub>sect</sub> ) below VREG (REGOR[7:2])           7         EN_TTERM         RW         By REG_RST By Watchdog         1         Onarging Termination Enable 0 Disable         1 Enable (default)           6         Reserved         R         N/A         Always reads 0	1	BATLOWV	R/W		1	0—2.8V 1—3.0V (c	lefault)
1         BQ_LERW         NW         By/Watchdog         1         0—Disable         1—Enable (default)           6         Reserved         R         N/A         Alwaysreads 0         Image: Comparison of the setting 0         Image: Comparisetion voltage Comp Above VREG (RE	0	VRECHG	R/W		0	(Below Cha 0—100m\	arge Voltage Limit) / (V <sub>RECHG</sub> ) below VREG (REG06[7:2]) (default)
1         B-LERW         N'W         By/Watchdog         1         0-Disable         1-Enable (default)           6         Reserved         R         N/A         Always reads 0         Image: Comparison of the setting 0           5         WATCHDOG[1]         R'W         By/REG_RST By Watchdog 0         Image: Comparison of the setting 0         Image: Comparison of the setting 0           4         WATCHDOG[0]         R'W         By/REG_RST By Watchdog 1         Image: Comparison of the setting 0         Image: Comparison of the setting 0           3         BN_TIMER         R'W         By/REG_RST By Watchdog 1         Image: Comparison of the setting 0         Image: Comparison of the setting 0           2         CHG_TIMER(1)         R'W         By/REG_RST By Watchdog 0         Image: Comparison of the setting 0         Image: Comparison of the setting 0           1         CHG_TIMER(1)         R'W         By/REG_RST By Watchdog 1         Image: Comparison of the setting 0         Image: Comparison of the setting 0           0         JETA_LISET (0°C-I0°C)         R'W         By/REG_RST By Watchdog 0         Som Ω         Image: Comparison feesitor Setting Range: Omage: Comp Above VREG (RECOG[7:2])           6 </td <td></td> <td></td> <td></td> <td></td> <td></td> <td>~</td> <td></td>						~	
5         WATCHDOQ[1]         RW         By REG_RST By Watchdog         0         I <sup>2</sup> CWatchdog Timer Setting 00—Dsable watchdog timer           4         WATCHDOG[0]         RW         By REG_RST By Watchdog         1         01—40s (default)           3         BN_TIMER         RW         By REG_RST By Watchdog         1         0—Dsable watchdog timer           2         CHG_TIMER[1]         RW         By REG_RST By Watchdog         1         0—Dsable 1—Enable (default)           1         CHG_TIMER[1]         RW         By REG_RST By Watchdog         1         0—Dsable 1—Enable (default)           1         CHG_TIMER[1]         RW         By REG_RST By Watchdog         1         Fas Charge Timer Setting 00—5 hrs           0         JETA_ISET By Watchdog         By REG_RST By Watchdog         0         JETA Low Temperature Current Setting 0—50% of ICHG (REG04[6:0]) (default)           7         BAT_COMF[2]         RW         By REG_RST By Watchdog         0         80mΩ           6         BAT_COMF[2]         RW         By REG_RST By Watchdog         0         20mΩ           5         BAT_COMF[2]         RW         By REG_RST By Watchdog         0         20mΩ           4         VCLAMF[2]         RW         By REG_RST By Watchdog         0         20mΩ		_		By Watchdog	1	0—Disable	e 1—Enable (default)
S         WAICHEOQ[1]         NW         By Watchdog         0         00-Disable watchdog timer           4         WATCHEOQ[0]         RW         By REG_RST By Watchdog         1         01-400 (default)         10-400 (default)           3         EN_TIMER         RW         By REG_RST By Watchdog         1         Oharging Safety Time Enable 0-Disable 1-Enable (default)           2         CHG_TIMER(1]         RW         By REG_RST By Watchdog         0         Targe Timer Setting 00-5 hrs         00-5 hrs           1         CHG_TIMER(0]         RW         By REG_RST By Watchdog         0         10-12 hrs (default)         11-10 hrs           0         JETA_ISET (0°C-10°C)         RW         By REG_RST By Watchdog         0         JETA Low Temperature Current Setting 0-50% of ICHG (REG04[6:0])         0-50% of ICHG (REG04[6:0])           6         BAT_COMIF[2]         RW         By REG_RST By Watchdog         0         80mΩ         IR Compensation Resistor Setting Range:0140mΩ           5         BAT_COMIF[1]         RW         By REG_RST By Watchdog         0         20mΩ         IR Compensation Voltage Camp Above VREG (REG06[7:2])           4         VCLAMIF[2]         RW         By REG_RST By Watchdog         0         32mV         IR Compensation Voltage Camp Above VREG (REG06[7:2])	6	Reserved	R				
4         WATCHDOG[0]         R'W         By REG_RST By Watchdog         1         1080s 11160s           3         BN_TIMER         R'W         By REG_RST By Watchdog         1         Oharging Safety Time Enable 0 - Disable         1         -Enable (default)           2         CHG_TIMER[1]         R'W         By REG_RST By Watchdog         1         Fast Charge Timer Setting 00-5 hrs         00-5 hrs           1         CHG_TIMER[0]         R'W         By REG_RST By Watchdog         0         JITA_ISET (0°C-10°C)         R'W         By REG_RST By Watchdog         0         JITA_IO hrs           0         JETA_ISET (0°C-10°C)         R'W         By REG_RST By Watchdog         0         JITA_ION Temperature Qurrent Setting 0-50% of ICHG (REC04[6:0]) 120% of ICHG (REC04[6:0])           6         BAT_COMIF[2]         R'W         By REG_RST By Watchdog         0         80mΩ         IR Compensation Resistor Setting Range:0-140mΩ Default:0Ω           5         BAT_COMIF[1]         R'W         By REG_RST By Watchdog         0         20mΩ           4         VCLAMIF[2]         R'W         By REG_RST By Watchdog         0         128mV         IR Compensation Voltage Qamp Above VREG (REC06[7:2]) Of Settint:0N           3         VCLAMIF[1]         R'W         By REG_RST By Watchdog         0         32mV<	5	WATCHDOG[1]	R∕W		0	00—Disab	le watchdog timer
3         EN_IMMER         RW         By/Watchdog         1         0Disable         1Enable (default)           2         CHG_TIMER(1)         RW         By/REG_RST By/Watchdog         1         0Disable         1Enable (default)           1         CHG_TIMER(0)         RW         By/REG_RST By/Watchdog         0         -S hrs         005 hrs           0         JETA_ISET (0°C-10°C)         R/W         By/REG_RST By/Watchdog         0         JETA Low Temperature Qurrent Setting 050% of ICHG (REG04[6:0])           0         JETA_ISET (0°C-10°C)         R/W         By/REG_RST By/Watchdog         1         JETA Low Temperature Qurrent Setting 020% of ICHG (REG04[6:0])           1        20% of ICHG (REG04[6:0])         120% of ICHG (REG04[6:0]) (default)         120% of ICHG (REG04[6:0]) (default)           6         BAT_COMP[1]         R/W         By/REG_RST By/REG_RST         0         80mΩ           5         BAT_COMP[0]         R/W         By/REG_RST By/REG_RST         0         20mΩ           4         VCLAMP[2]         R/W         By/REG_RST By/REG_RST         0         128mV         IR Compensation Voltage Camp Above VREG (REG06[7:2])         Above VREG (REG06[7:2])         0fset:0mV         Rage:0224mV         Default:0mV         2         VCLAMP[0]         R/W <t< td=""><td>4</td><td>WATCHDOG]0[</td><td>R/W</td><td></td><td>1</td><td colspan="2" rowspan="2">10—80s 11—160s Charging Safety Time Enable</td></t<>	4	WATCHDOG]0[	R/W		1	10—80s 11—160s Charging Safety Time Enable	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	3	EN_TIMER	R/W		1		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	2	CHG_TIMER[1]	R/W		1		e Timer Setting
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	1	CHG_TIMER[0]	R/W		0	10—12 hr:	
7       BAT_COMP[2]       R/W       By Watchdog       0       80m2       IR Compensation Resistor Setting         6       BAT_COMP[1]       R/W       By REG_RST       0       40mΩ       Range:0-140mΩ       Default:0Ω         5       BAT_COMP[0]       R/W       By REG_RST       0       20mΩ       Default:0Ω       Default:0Ω         4       VCLAMP[2]       R/W       By REG_RST       0       128mV       IR Compensation Voltage Camp Above VREG (REG06[7:2])         3       VCLAMP[1]       R/W       By REG_RST       0       64mV       Offset:0mV         2       VCLAMP[0]       R/W       By REG_RST       0       32mV       Default:0mV         1       TREC[1]       R/W       By REG_RST       0       32mV       Default:0mV         1       TREC[1]       R/W       By REG_RST       0       32mV       Default:0mV         0       Thermal Regulation Threshold       00-60°C       01-80°C       01-80°C         0       TREC[1]       R/W       By REG_RST       1       10-100°C	0		R/W	· -	1	0—50%of	ICHG (REG04[6:0])
7       BAT_COMP[2]       R/W       By Watchdog       0       80m2       IR Compensation Resistor Setting         6       BAT_COMP[1]       R/W       By REG_RST       0       40mΩ       Range:0-140mΩ       Default:0Ω         5       BAT_COMP[0]       R/W       By REG_RST       0       20mΩ       Default:0Ω       Default:0Ω         4       VCLAMP[2]       R/W       By REG_RST       0       128mV       IR Compensation Voltage Camp Above VREG (REG06[7:2])         3       VCLAMP[1]       R/W       By REG_RST       0       64mV       Offset:0mV         2       VCLAMP[0]       R/W       By REG_RST       0       32mV       Default:0mV         1       TREC[1]       R/W       By REG_RST       0       32mV       Default:0mV         1       TREC[1]       R/W       By REG_RST       0       32mV       Default:0mV         0       Thermal Regulation Threshold       00-60°C       01-80°C       01-80°C         0       TREC[1]       R/W       By REG_RST       1       10-100°C							
6       BAT_COMIF[1]       R'W       By REG_RST By Watchdog       0       40mΩ       Rage:0-140mΩ Default:0Ω         5       BAT_COMIF[0]       R'W       By REG_RST By Watchdog       0       20mΩ       IR Compensation Voltage Camp Above VREG (RECOG[7:2])         3       VCLAMIF[1]       R'W       By REG_RST By Watchdog       0       64mV       Offset:0mV Range:0-224mV       Offset:0mV Default:0mV         2       VCLAMIF[0]       R'W       By REG_RST By Watchdog       0       32mV       Offset:0mV Default:0mV         1       TREC[1]       R'W       By REG_RST By Watchdog       0       32mV       Default:0mV         1       TREC[1]       R/W       By REG_RST By Watchdog       1       Thermal Regulation Threshold 00-60°C         0       TREC[1]       R/W       By REG_RST By Watchdog       1       Thermal Regulation Threshold 00-60°C	7	BAT_COMP[2]	R/W	By Watchdog	0	80mΩ	IR Compensation Resistor Setting
5     BAT_COMIP[0]     R'W     By REG_RST By Watchdog     0     20mΩ       4     VCLAMIP[2]     R'W     By REG_RST By Watchdog     0     128mV     IR Compensation Voltage Camp Above VREG (REC06[7:2])       3     VCLAMIP[1]     R'W     By REG_RST By Watchdog     0     64mV     Offset:0mV Range:0224mV       2     VCLAMIP[0]     R'W     By REG_RST By Watchdog     0     32mV     Default:0mV       1     TREC[1]     R'W     By REG_RST By Watchdog     1     Thermal Regulation Threshold 00-60°C       0     TREC[1]     R/W     By REG_RST By REG_RST     1     Thermal Regulation Threshold 00-60°C	6	BAT_COMP[1]	R/W	By Watchdog	0	40mΩ	Range:0—140mΩ
4       VCLAWIP[2]       R/W       By Watchdog       0       128mV       IR Compensation Voltage Damp         3       VCLAMIP[1]       R/W       By REG_RST       0       64mV       Above VREG (REG06[7:2])         2       VCLAMIP[0]       R/W       By REG_RST       0       32mV       Offset:0mV         1       TREC[1]       R/W       By REG_RST       0       32mV       Default:0mV         1       TREC[1]       R/W       By REG_RST       1       Thermal Regulation Threshold         0       TREC[1]       R/W       By REG_RST       1       Thermal Regulation Threshold         0       TREC[1]       R/W       By REG_RST       1       Thermal Regulation Threshold	5	BAT_COMP[0]	R∕W	By Watchdog	0	20mΩ	
3     VCLAMP[1]     R/W     By REG_RST By Watchdog     0     64mV     Offset:0mV     Rage:0-224mV       2     VCLAMP[0]     R/W     By REG_RST By Watchdog     0     32mV     Default:0mV       1     TREG[1]     R/W     By REG_RST By Watchdog     1     Thermal Regulation Threshold 00-60°C       0     TREG1     R/W     By REG_RST By REG_RST     1     Thermal Regulation Threshold 00-60°C	4	VOLAMP[2]	R∕W	By Watchdog	0	128mV	
2     VCLAMP[0]     R/W     By REG_RSI By Watchdog     0     32mV     Default:0mV       1     TREG[1]     R/W     By REG_RST By Watchdog     1     Thermal Regulation Threshold 00-60°C       0     TREG1     By REG_RST By REG_RST     1     Thermal Regulation Threshold 00-60°C       0     TREG1     By REG_RST By REG_RST     1	3	VCLAMP[1]	R∕W	By Watchdog	0	64mV Offset:0mV	
I         INCUIT         INV         By Watchdog         I         00—60°C           0         TRECT         By REG_RST         01—80°C           0         TRECT         By REG_RST         10—100°C	2	VCLAMP[0]	R∕W	By Watchdog	0		Default:0mV
D TREGI BY REG_RST 1 10-100°C	1	TREG[1]	R/W	· -	1	00-60°C	egulation infeshold
By Watchdog 11—120°C (default)	0	TREG[]	R/W	By REG_RST By Watchdog	1	10—100°0	



7	FORCE_ICO	₽₩	By REG_RST By Watchdog	0	Force Start Input Current Optimizer 0—Do not force ICO (default) 1—Force ICO Note: This bit is can only be set only and always return to 0 after ICO starts
6	TMR2X_EN	R/W	By REG_RST By Watchdog	1	Safety Timer Setting During DPM or Thermal Regulation 0—Safety time not slowed by 2X during DPM or thermal regulation 1—Safety time slowed by 2X during DPM or thermal regulation (default)
5	BATFET_DIS	R∕W	By REG_RST	0	Force BATFET off to enable ship mode 0—Allow BATFET turn on (default) 1—Force BATFET off
4	JEITA_VSET (45°C—60°C)	R∕W	By REG_RST By Watchdog	0	JETA High Temperature Voltage Setting 0—Setting charging voltage to VREG-200mV during JETA high temperature 1—Setting charging voltage to VREG during JETA high temperature
3	BATFET_DLY	R∕W	By REG_RST	0	BATFET Turn Off Control 0—BATFET turn off immediately when BATFET_DISbit is set 1—BATFET turn off delay t <sub>SM_DLY</sub> when BATFET_DISbit is set
2	BATFET_RST_ EN	R/W	By REG_RST	1	BATFET Full System Reset Enable 0—Disable BATFET full system reset 1—Enable BATFET full system reset
1	PUMPX_UP	₽₩	By REG_RST By Watchdog	0	Ourrent Pulse Control Voltage UP enable 0—Disable (default) 1—Enable Note: This bit can only be set when EN_PUMPX bit is set and return to 0 after current pulse control sequence is complete
0	PUMPX_DN	R/W	By REG_RST By Watchdog	0	Current Pulse Control Voltage Down enable         0—Disable (default)         1—Enable         Note:         This bit can only be set when EN_PUMPX bit is set and return to 0 after current pulse control sequence is complete
7	Reserved	R	N/A		Always reads 0
6	Reserved	R	N/A		Always reads 0
5	Reserved	R	N/A		Always reads 0
4	Reserved	R	N/A		Always reads 0
3	Reserved	R	N/A		Always reads 0
2	Reserved	R	N/A		Always reads 0
1	Reserved	R	N/A		Always reads 0
0	Reserved	R	N/A		Always reads 0



7							
	VBUS_STAT[2]	R	N/A	N/A	VBUS Statues Register		
6		R	N/A	N/A	000: No Input		
-		TX .	1071	1.0/7	001:USB Host SDP		
		_			010:Adapter (3.25A)		
5	VBUS_STAT[0]	R	N/A	N/A	111:OTG		
					Note: Software current limit is reported in IINLIM register		
4	CHRG_STAT[1]	R	N/A	N/A	Charging Status		
			-		00—Not charging		
					01—Pre-charge ( <v<sub>BATLOW)</v<sub>		
3	CHRG_STAT[0]	R	N/A	N/A	10—Fast charging		
					11—Charge Termination Done		
					Power Good Status		
2	PG_STAT	R	N/A	N/A	0—Not Power good		
2		IX.			1—Power good		
- 1	Deserved	D	N/A	0			
1	Reserved	R	IN/ A	0	Always reads 0		
		<b>_</b>	NI/ A	N1/ A	VSYSRegulation Status		
0	VSYS_STAT	R	N/A	N/A	0—Not in VSYS_MIN regulation		
					1—In VSYS_MIN regulation		
_	WATCHDOG	-			Watchdog Fault Status		
7	FAULT	R	N/A	1	0—Normal		
		_			1—Watchdog timer expiration (default)		
6		R	N/A	N/A	Always reads 0		
5	CHRG_FAULT[1]	R	N/A	N/A	Charge Fault Status		
4	CHRG_FAULT[0]	R	N/A	N/A	01—Input fault (VBUS>V <sub>ACOV</sub> or VBAT <vbus<v<sub>VBUSMIN (typical 3.8V)</vbus<v<sub>		
	0				10—Thermal shut down		
					11—Charge safety timer expiration		
3	BAT_FAULT	R	N/A	N/A	Battery Fault Status		
	_		-		0—Normal 1—BATOVP (V <sub>BAT</sub> >V <sub>BATOVP</sub> )		
2		R	N/A	N/A	NTC Fault Status		
1	NTC_FAULT[1]	R	N/A	N/A	Buck Mode:		
					000—Normal		
					010—THM warm		
0	NTC_FAULT[0]	R	N/A	N/A	011—THM cool		
					101—THM cold		
					110—THM hot		
					VINDPM Threshold Setting Method		
7	FORCE_VINDPM	R/W	By REG_RST	0	0—Run relative VINDPM threshold (default)		
					1-Run absolute VINDPM threshold		
6	VINDPM[6]	R/W	By REG_RST	0	6400mV Absolute VINDPM threshold		
5	VINDPM[5]	R∕W	By REG_RST	0	3200mV Offset:2.6V		
4	VINDPM[4]	R∕W	By REG_RST	1	1600mV Range:3.9V(0001101)—15.3V(1111111)		
3	VINDPM[3]	R∕W	By REG_RST	0	800mV Note:		
2		R/W	By REG_RST	0	400mV Value<0001101 is clamped to 3.9V		
1		R/W	By REG_RST	1	200mV Register is read only when FORCE_VINDPM=0 and can be		
					written by internal control based on relative VINDPM threshold		
0	VINDPM[0]	R/W	By REG_RST	0	100mV setting		
0					Register can be read/write when FORCE VINDPM=1		



					Thermal R	Regulation Status
7	THERM_STAT	R	N/A	N/A	0—Norma	
						mal regulation
6	BATV[6]	R	N/A	0	1280mV	
5	BATV[5]	R	NA	0	640mV	
4	BATV[4]	R	N/A	0	320mV	ADC Conversion of Battery Voltage (V <sub>BAT</sub> )
3	BATV[3]	R	N/A	0	160mV	Offset:2.304V
2	BATV[2]	R	N/A	0	80mV	Range:2.304V(000000)—4.848V(111111)
1	BATV[1]	R	N/A	0	40mV	Default:2.304V(000000)
0	BATV[0]	R	N/A	0	20mV	
7	Reserved	R	N/A	0	Always rea	ads 0
6	VSY9[6]	R	N/A	0	1280mV	
5	VSY9[5]	R	N/A	0	640mV	
4	VSY9[4]	R	N/A	0	320mV	ADC Conversion of System Voltage (V <sub>S/S</sub> )
3	VSY9[3]	R	N/A	0	160mV	Offset:2.304V
2	VSYS[2]	R	N/A	0	80mV	Range:2.304V(0000000)—4.848V(1111111)
1	VSYS[1]	R	N/A	0	40mV	Default:2.304V(0000000)
0	VSYS[0]	R	N/A	0	20mV	
7	Reserved	R	N/A	0	Always rea	ads 0
6	TSPCT[6]	R	N/A	0	29.76%	
5	TSPCT[5]	R	N/A	0	14.88%	ADC Conversion of $\pi M / (altern () / )$ on Demonstrate of )/
4	TSPCT[4]	R	N/A	0	7.44%	ADC Conversion of THM Voltage ( $V_{THM}$ ) as Percentage of $V_{LDO}$
3	TSPCT[3]	R	N/A	0	3.72%	Offset:21% Range:21%(0000000)—80%(1111111)
2	TSPCT[2]	R	N/A	0	1.86%	Default:21%(0000000)
1	TSPCT[1]	R	N/A	0	0.93%	Derault.21%(000000)
0	TSPCT[0]	R	N/A	0	0.465%	
					VBUSGoo	
7	VBUS GD	R	N/A	N/A		BUSAttached
'	1000_00			1.07.1	1-VBUS	
					VBUS_GD	
6	VBUS[6]	R	N/A	0	6400mV	
5	VBUS[5]	R	N/A	0	3200mV	ADC conversion of VBUS Voltage
4	VBUS[4]	R	N/A	0	1600mV	Offset: 2.6V
3	VBUS[3]	R	N/A	0	800mV	Range: 2.6V (0000000) 15.3V (1111111)
2	VBUS[2]	R	N/A	0	400mV	Default: 2.6V
1	VBUS[1]	R	N/A	0	200mV	
0	VBUS[0]	R	N/A	0	100mV	
7	Unused	R	N/A	0	Always Re	ads 0
6	ICHGR[6]	R	N/A	0	3200mA	ADC Conversion of Charge Current (IBAT) when VBAT>VBATSHORT
5	ICHGR[5]	R	N/A	0	1600mA	Offset:0mA
4	ICHGR[4]	R	N/A	0	800mA	Range:0mA(0000000)—6350mA(1111111)
3	ICHGR[3]	R	N/A	0	400mA	Default:0mA(0000000)
2	ICHGR[2]	R	N/A	0	200mA	Note:
1	ICHGR[1]	R	N/A	0	100mA	This register returns 0000000 for VBAT <vbatshort< td=""></vbatshort<>
0	ICHGR[0]	R	N/A	0	50mA	



					VINDPM S	totuo
7		<b>D</b>	NI/ A	NI/ A	0—Not in	
7	VDPM_STAT	R	N/A	N/A	1—In VIN	
		_			IINDPM St	
6	IDPM_STAT	R	N/A	N/A	0—Not in	
-					1—In IINE	PM
5	IDPM_UM[5]	R	N/A	0	1600mA	
4	IDPM_UM[4]	R	N/A	0	800mA	Input Ourrent Limit in Effect while Input Ourrent Optimizer
3	IDPM_LIM[3]	R	N/A	0	400mA	(ICO) is enabled
2	IDPM_LIM[2]	R	N/A	0	200mA	Offset:100mA
1	IDPM_LIM[1]	R	N/A	0	100mA	Range:100mA(000000)—3.25A(111111)
0	IDPM_LIM[0]	R	N/A	0	50mA	
				Register Reset		eset
					0—Keep c	surrent register setting
7	REG_RST	R/W	N/A	0	1-Reset t	to default register value and reset safety timer
					Note:	
					Reset to 0	after register reset is completed
					Input Curr	ent Optimizer (ICO) Status
6	ICO_OPTIMIZED	R	N/A	N/A	0-Optim	ization is in progress
	_				1-Maxim	num input current detected
5	PN[2]	R∕W	N/A		<u> </u>	
4	PN[1]	R∕W	N/A		Device cor	
3	PN[0]	R/W	N/A		000:OZ1O	32
2		R/W	N/A	1	Temperature Profile	
2	TS_PROFILE	.,		1	1-JETA	
1	DEV_REV[1]	R/W	N/A			<i>l</i> ision:01
0	DEV_REV[0]	R/W	N/A		Device Revision:01	



### TYPICAL APPLICATION SCHEMTAIC

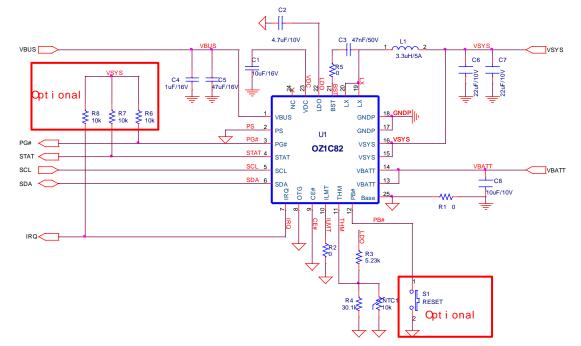


Figure 15: OZ1C82 Typical Application Schematic

#### **BILL OF MATERIALS**

Item	Qty	Reference	Value	Vendor	Part Number	PCB Footprint
1	1	C1	10µF/16V	Any	Ceramic – X7R or X5R	0805
2	1	C2	4.7µF/10V	Any	Ceramic – X7R or X5R	0805
3	1	C3	47nF/50V	Any	Ceramic – X7R or X5R	0603
4	1	C4	1µF/16V	Any	Ceramic – X7R or X5R	0603
5	1	C5	47µF/16V	Any	Ceramic – X7R or X5R	0805
6	2	C6,C7	22µF/10V	Any	Ceramic – X7R or X5R	0805
7	1	C8	10µF/10V	Any	Ceramic – X7R or X5R	0805
8	2	R1,R2	Ω0	Any	-	0603
9	1	R3	5.23kΩ 1%	Any	-	0603
10	1	R4	30.1kΩ1%	Any	-	0603
11	1	R5	0Ω	Any	-	0603
12	3	R6,R7,R8	10kΩ	Any	-	0603
13	1	NTC	103AT	-	-	0603
14	1	L1	3.3µH/5A	Würth Elektronik	74437346033	7.3x6.6x2.8
15	1	U1	-	O2Micro, Inc.	OZ1C82	QFN24 4mmx4mr



#### **COMPONENT SUPPLIERS**

Manufactura	Contact	Information
Manufacturer	Phone	Website
Inductors		
Würth Elektronik	+49 (0) 79 42 945 -5000	http://www.we-online.com
Capacitors		
Vishay	1-847-803-6100	www.vishay.com
Johanson Dielectrics	1-818-364-9800	www.johansondielectrics.com
TDK	1-800-344-2112	www.tdk.com
SANYO	N/A	http://www.sanyo.com/components/
Würth Elektronik	+49 (0) 79 42 945 -5000	http://www.we-online.com
Resistors		
Vishay	1-402-563-6866	www.vishay.com
TDK	1-800-344-2112	www.tdk.com

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